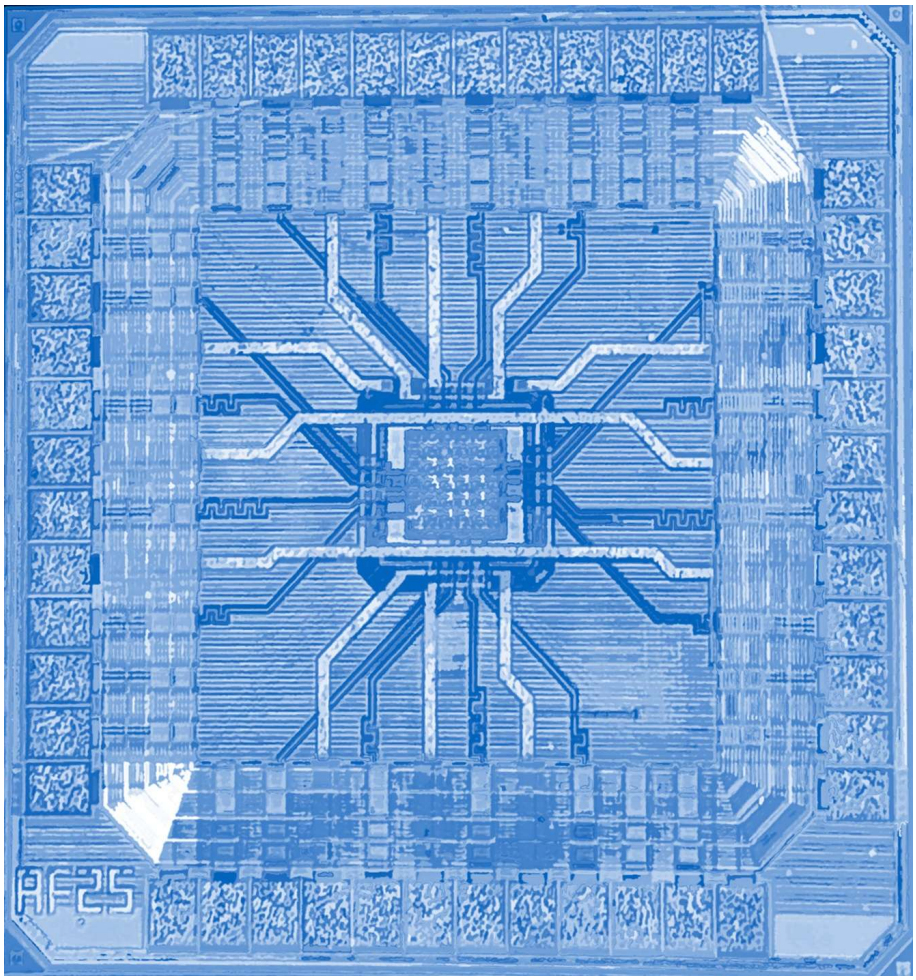
TECHNISCHE UNIVERSITÄT MÜNCHEN

TUM School of Natural Sciences

Bachelor's Thesis

Development of a novel silicon detector using CMOS technology

Alexander Musta



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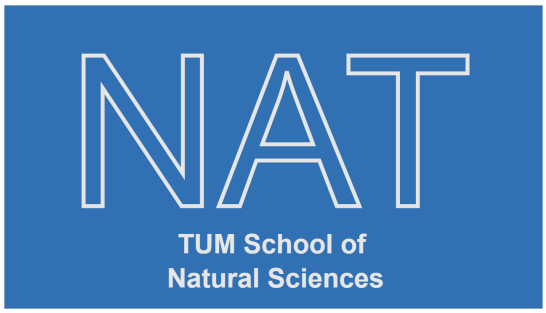

Development of a novel silicon detector using CMOS technology

Entwicklung eines neuen Silizium Detektors mit der CMOS Technologie

Bachelor's Thesis

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Date:	22.08.2023

I confirm that the results presented in this bachelor's thesis are my own work, and I have documented all sources and materials used.

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Munich, 22.08.2023 Alexander Musta

Abstract

This work discusses the Analog Pixel Testing Structure (APTS) used to test different pixel designs for the upcoming new Inner Tracking System (ITS3) for the ALICE experiment. The underlying motivation for testing these pixel technologies is to find the most suitable silicon detector which minimizes charge sharing, power consumption, and data output. The already existing ALICE Pixel Detector (ALPIDE) is a Monolithic Active Pixel Sensor (MAPS) utilizing CMOS technology. For the ITS3, MAPS detectors are envisioned. Different doping structures and pixel sizes are currently under investigation.

In this thesis, the most promising doping layout, called modified process with a gap for different pixel sizes, has been investigated. Properties such as capacitance, charge collection efficiency (CCE), mean cluster sizes, and the behavior under different bias voltages for these chips has been studied. To characterize these silicon chips, measurements from an ^{55}Fe source inside the laboratory have been taken.

In addition, the energy calibration of the chip is investigated. The total linearity between the deposited energy and signal inside of the detector has been studied. For the energy calibration, another radioactive source, ^{41}Ca, has been used as well. Lastly, the effect of the threshold on the cluster size distribution has been analyzed.

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6 Summary **30**

1. Introduction

At the Large Hadron Collider (LHC), located at CERN in Switzerland, high-energy particles collide in order to allow us to study the fundamental building blocks of matter. The upcoming High-Luminostiy Large Hadron Collider project will be a substantial upgrade to the existing LHC and its detector systems. This project aims to increase the luminosity to get higher statistics on processes with very low probabilities, such as the creation of the Higgs Boson. It will include additional quadrupole magnets for the ATLAS and CMS experiments, superconducting links for electrical transmission, and many additional features [1]. A rough overview of some new technologies which will be implemented in the LHC-HL is shown in Figure 1. These upgrades will be implemented in 2026 as the LHC will shut down for a third time (Large Shutdown LS 3) [2].

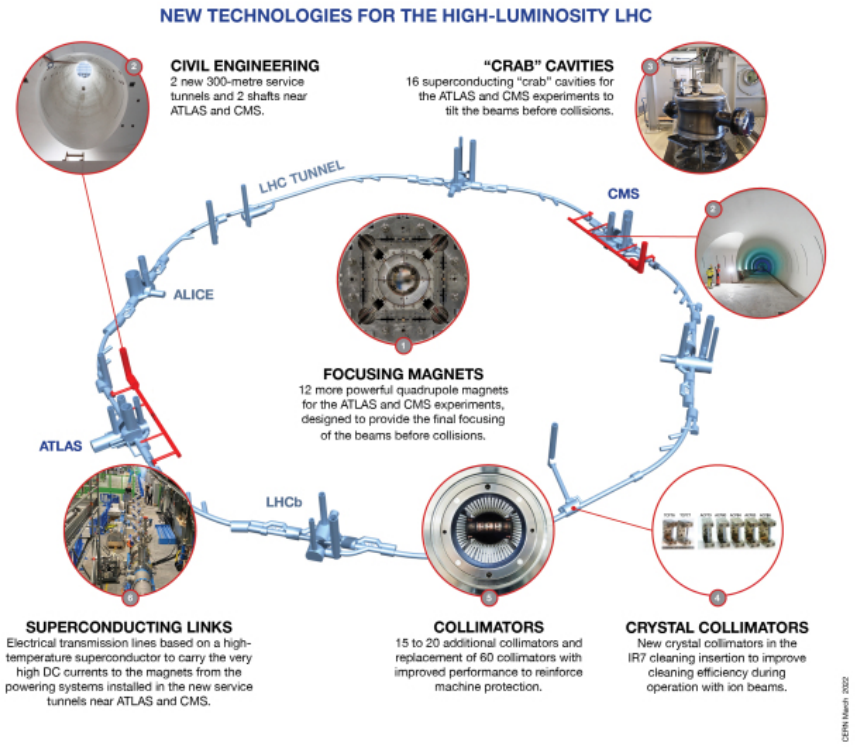


Figure 1 An overview on the new technologies which will be incorporated for the LHC-HL project [1]

At the "A Large Ion Collider Experiment" (ALICE), heavy ion collisions, such as lead-lead collisions, are used to study the effects of the strong interaction at high energies. At the achieved energy densities, a new phase of matter arises, the so-called quark-gluon plasma, which is assumed to be formed right after the Big Bang [4]. The ALICE experiment, see Figure 2, like other experiments at the LHC, will undergo upgrades to its detector systems. A higher vertex resolution aims to distinguish between two very close tracks coming out from the interaction point. Such improvements may enable us to understand better high-precision beauty measurements, $D\overline{D}$ correlation, measurements of multi-charm baryons and exotic hadrons, etc. [5].

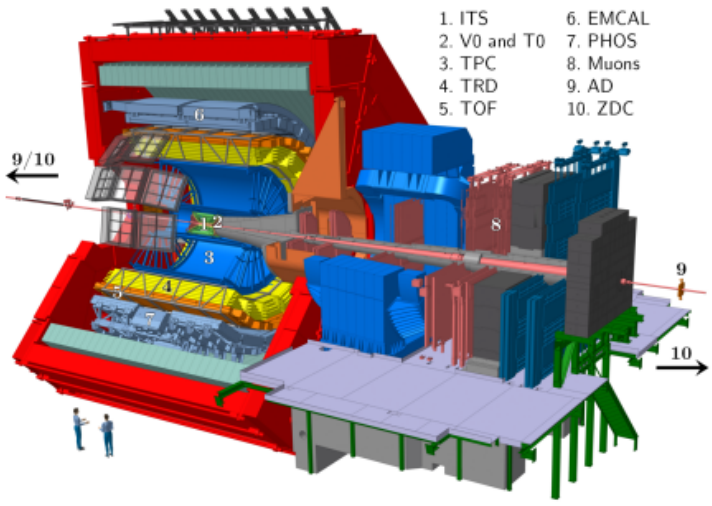


Figure 2 The ALICE detector system [3]

The already operational Inner Tracking System (ITS2) consists of tracking detectors closest to the interaction point and is based on the Monolithic Active Pixel Sensor (MAPS) technology. Its major advantage is a continuously active low-power front-end placed in each pixel, which allows for an extremely low detection noise and a data reduction already at this stage [6]. The ITS2 is scheduled for upgrade and will get replaced by a new tracking detector system (ITS3) for run 4 at the LHC scheduled around 2029. Like the ITS2, this detector system will also be based on MAPS. The pixel technology for the ITS3 is currently under study in terms of different pixel doping structures and sizes. This thesis will cover the Analog Pixel Testing Structure (APTS), introduced in the section 4, used to test these different pixel architectures and elaborate on measurements taken from radioactive sources in the laboratory.

2. The ALICE Inner Tracking System

2.1. The ITS2

The ALICE Inner Tracking System consists of detectors shaped into barrels in order to cover a nearly 4π angle around the interaction point. The barrel section is distributed into Inner Barrel (IB) and Outer Barrel (OB), including three and four layers of MAPS detectors, respectively; see Figure 3.

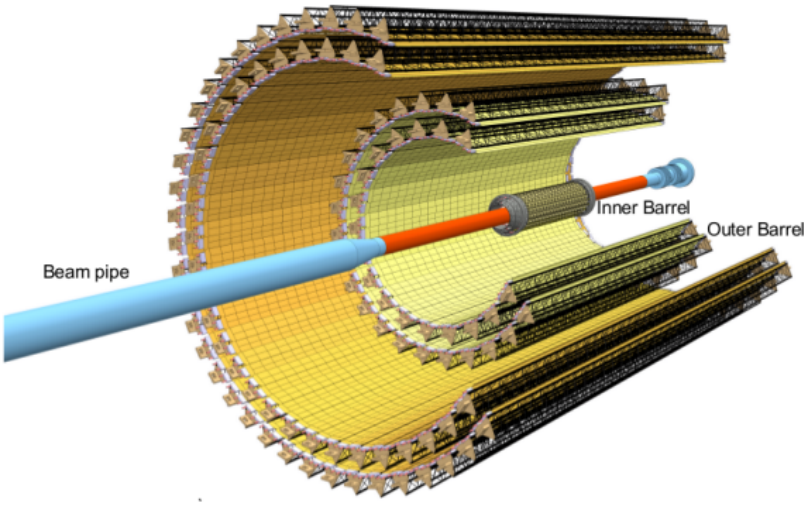


Figure 3 ITS2 layout: The Inner Barrel (IB) consists of 3 layers and the Outer Barrel (OB) consists of 2 middle layers and 2 outer layers [7]

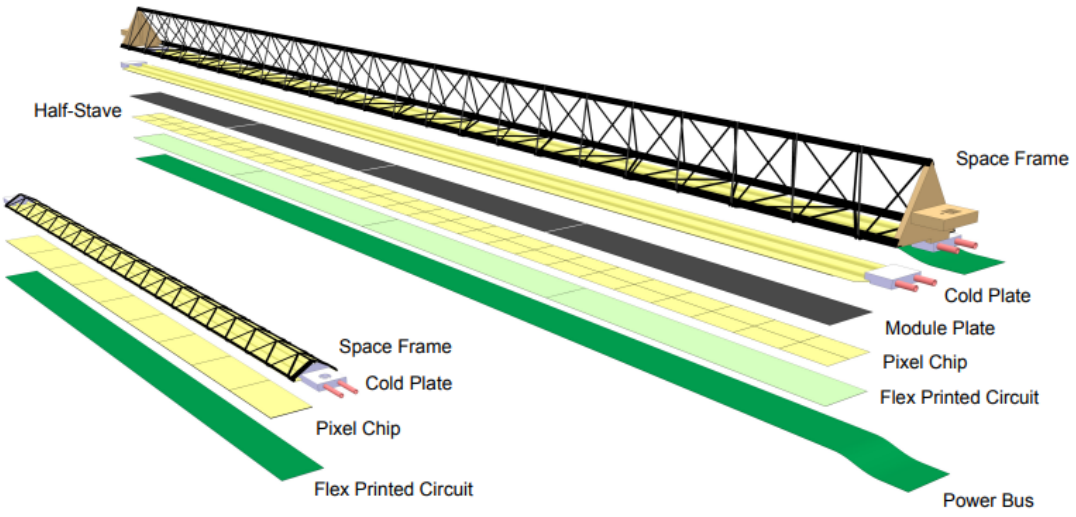


Figure 4 Stave structure for the Inner Barrel (left) and half-stave for the outer barrels (right) [8, p.9]

Each layer is built up of so-called staves. The staves for the Inner Barrel, see left panel on

Figure 4, comprise a space frame for mechanical stability, a cold plate providing necessary cooling, and the pixel chip itself. The ITS2 detectors are cooled by water, impacting the material budget; see Figure 5. The pixel chips are based on Monolithic Active Pixel Sensors (Section 3), and a Flex Printed Circuit (FPC) provides the necessary electrical infrastructure to the chip. The pixel chip and FPC form a Hybrid Integrated Circuit (HIC). For the outer barrels, each stave is segmented in two halves azimuthally. In addition, the outer barrels are longitudinally divided into modules. These modules are Hybrid Integrated Circuits glued to a carbon-based Module Plate. An additional bus is needed to provide power to the detectors for the outer barrels (Power Bus) [8]. It should be noted that the Inner Barrel staves are slightly overlapping, shown on the right panel of Figure 6. The stave geometry supports a planar detector layer, which does not fully account for the cylindrical shape of the beam pipe (see Figure 3).

2.1.1. Material Budget

This section discusses the importance of the material budget. An increase in the material budget leads to increased multiple scattering of the particles from the interaction and the detector material, altering the trajectories of the particles. In addition, secondary reactions in the detector material create a background reducing the efficiency of the detector and increasing the data load for the outer detector systems. Therefore, the material budget should be kept as low as possible.

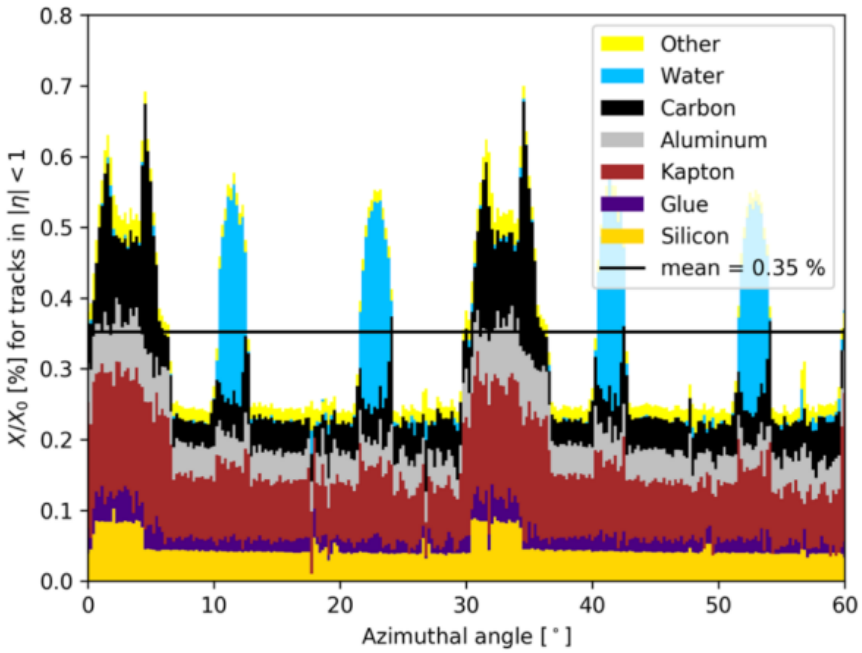


Figure 5 Material budget for the Inner Barrel Layer 0: Azimuthal distribution [9, p.7]

Figure 5 shows the material budget of the building blocks of ITS2 Inner Barrel in units of radiation length plotted against the azimuthal angle. This material budget exhibits a non-uniform distribution characterized by periodic peaks. The peaks in blue correspond to the coolant for the detector (cooling pipes filled with water). The peaks in black (Carbon) indicate

the overlap of the mechanical structures of two staves, illustrated on the left panel of Figure 6. A remarkable contribution to the total material budget is the Kapton foil, used to isolate the power of the FPC from the pixel detectors. The FPC contributes to about 50%, the cooling around 20%, and the mechanical support 15% of the total material budget [9]. In this case, the thickness of the detectors (silicon) is already low (roughly $50\,\mu\text{m}$) and contributes less than 15 % to the overall budget.

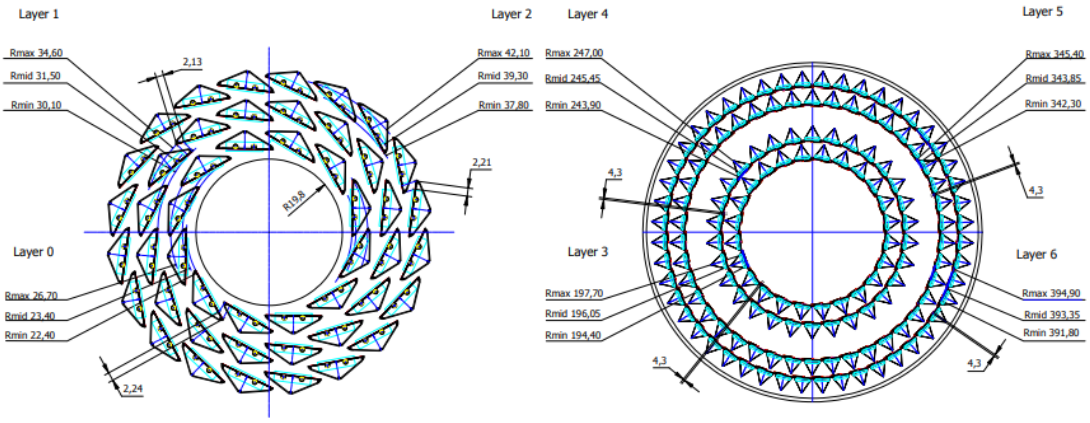


Figure 6 Crosssection of the Inner Barrel staves (left) and Outer Barrel staves (right). Overlap of each stave in the Inner Barrel is visible [8, p.8]

2.2. The ITS3

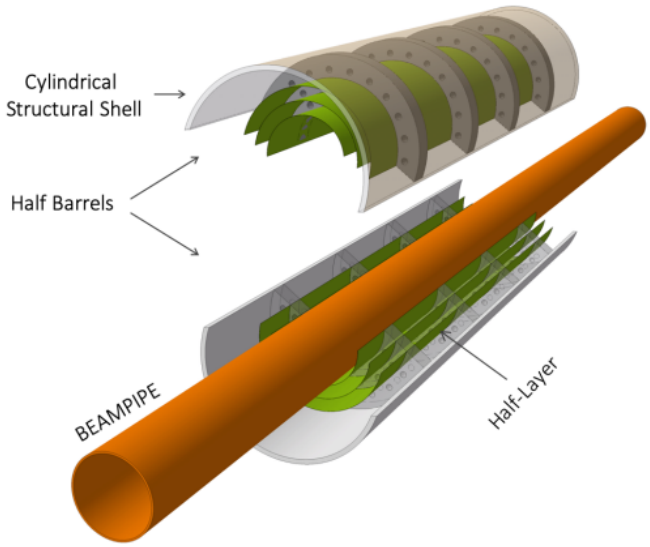


Figure 7 Schematic of the ITS3 Inner Barrel. Sensors are bent into three layers of half-barrels [9, p.10], supported by a low-mass mechanical structure made from carbon foam

For the upcoming third long LHC shutdown LS 3, beginning in 2026 [2], a new inner-tracker for the ALICE experiment, the ITS3, is foreseen to be installed. The Inner Barrel of the ITS2

will be replaced by 3 cylindrical detector layers; see Figure 7. The geometrical dimensions of the new Inner Barrel are shown in Table 1 [9]. The Inner Barrel will be installed closer to the interaction point, further improving the pointing resolution. For this reason, the beampipes will also be replaced.

Beampipe inner/outer radius (mm)	$16.0/16.5$		
IB Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	270	270	270
Pixel sensors dimensions (mm^2)	280×56.5	280×75.50	280×94
Pixel size (µm^2)	$\mathcal{O}(15 \times 15)$		

Table 1 Geometrical parameters of the ITS3 Inner Barrel [9, p.12]

Silicon detectors thinned down to 20-40 µm become flexible and can be bent to a cylindrical geometry. Initial studies using the 50 µm thick ALPIDE Chips have shown that bending silicon for the given thickness is possible as well as the performance of the bent ALPIDE chips did not decrease after bending ([10], [11]). Due to the mechanical property of the silicon wafers, fewer mechanical support structures are needed. For the ITS3 Inner Barrel, a lightweight half-wheel spacer made of carbon foam is used. The outer cylindrical structural shell also provides additional mechanical stability. The new detector will be cooled using a gas flow, reducing the material budget further.
The new technology of large area bent sensors also needs a new technology in producing the sensors, which have to reside on a single large area silicon wafer, not being cut into smaller units like the ALPIDE. For the manufacturing of these silicon chips, optical lithography is used. A thin photoresist film gets applied after preparing the substrate. Different patterns, called masks, can be brought onto the wafer via so-called Projection Printing on the photoresist film. In this case, lenses (or mirrors) project the intended relief onto the photoresist. The area at which light has been exposed becomes soluble and can be dissolved in the next manufacturing steps [12]. The area at which such structures can be printed is limited by the field of view of the optics used for manufacturing. Therefore only a small reticle of chips can be structured at once. Typically these units are cut out to be used as independent detector elements. To create bigger and interconnected chips, a new lithographic process will be used for the silicon detector in ITS3 called stitching [13]. In this process, the additional structures at the edges of the reticles are created to connect the units to the outside (cf. Figure 9). This allows for each reticle to be connected, "stitched," together. With that technology, wafer-scale chips can be produced [14].

A possible implementation of the stitching process for the ALICE ITS3 upgrade is illustrated in Figure 8. On the right-hand side, the geometric arrangement of different basic units for the chip on a silicon wafer is shown. On the left side, a possible architecture of such a chip

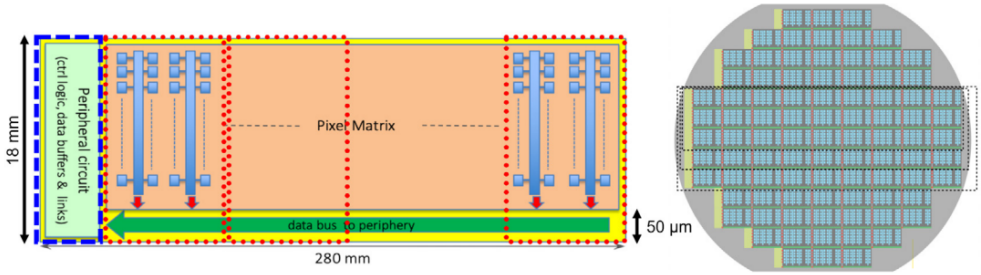


Figure 8 Left panel: Sketch of a possible implementation of stitched wafer-scale sensors. The periphery, indicated via blue dashed lines, and the pixel matrix, marked with red dashed lines, are shown. Right panel: Silicon wafer at which the detector is made, dotted lines indicate different ways the structures can get diced [10]

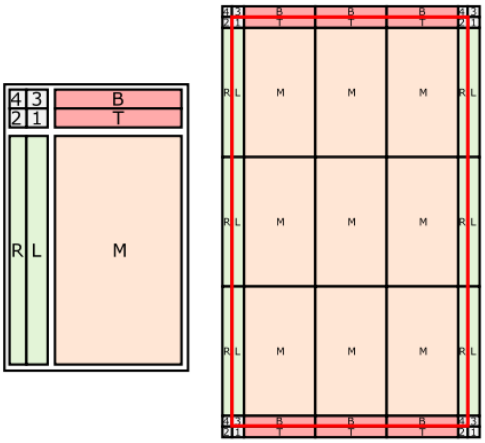


Figure 9 An example for the stitching manufacturing process: Reticle design is subdivided into smaller areas, seen on the left panel. In this case, M is the individual sensor area, and R, L, B, and T comprise the periphery. These structures are repeated, comprising one detector on the wafer, seen on the right panel. The red line indicates where the wafer gets cut [14]

is shown in which the pixel matrices are stitched together (each sub-matrix is marked with dashed lines in red in Figure 8), where a data bus periphery can transport the information to the peripheral circuit intended for readout, communication, regulation of voltages/currents, etc. [10]. This novel design makes the FPC board obsolete because all functionalities are already implemented inside the main chip. The prototypes of these stitched sensors are already designed and currently under production ([10],[14]). With these implementations, the distribution of the material budget becomes more homogenous, and the overall material budget shrinks to 0.05% X_0 per layer, about 1/7-th of the ITS2 [9]. In addition, the sensors will be optimized and manufactured using the 65 nm CMOS imaging process of Tower Semiconductor [15]. By utilizing smaller feature sizes of the transistors, more circuitry can be implanted on the active layer of the chip, and also the average power consumption can be further reduced. Different designs of the pixel layouts with varying sizes are under investigation using test structures striving for minimal charge sharing [1] and optimal detection efficiency, radiation hardness, and readout rate. A minimized charge sharing helps to decrease the output rate of the final detector, thereby decreasing the power for data transmission.

[1] Charge sharing refers to the charge created by an incident particle being detected by multiple pixels.

3. Monolithic Active Pixel Sensors (MAPS)

3.1. General remarks

Monolithic active pixel detectors incorporate the required circuitry for amplification, readout, discrimination, etc., using CMOS technology built on each pixel. This reduces the material budget by eliminating the need for a separate PCB board for the required electronics but especially minimizes the power consumption. For high-energy physics, a maximized performance with reduced power consumption is essential. By minimizing power consumption, one also reduces the materials needed for power supply and reduces the amount of cooling required [16].

In general, pixel detectors are diodes operated in reverse bias mode. Two charge collection mechanisms can occur: diffusion and drift. When an incident particle passes through the detector material creating free charge carriers outside of the depletion zone, the generated charge starts to diffuse inside the silicon. This is called diffusion current. The drift current is defined by the generated charge inside of the depletion zone, which can be increased by an external electric field [17, p. 452-460]. To optimize charge collection in the detector, a large depletion zone is needed in which the electrons undergo drift guided by the electric field inside the silicon. This results in a faster charge collection and in reduced charge sharing between adjacent pixels than in the case of diffusion. For diffusion, it is prone to be trapped by defects inside the crystal, which eventually results in a loss of signal amplitude. Suppose the crystal has been damaged by radiation. In that case, this process is much more likely to happen due to the higher concentration of defects, therefore resulting in a lower radiation tolerance [16]. A silicon sensor should have a high so-called Q/C ratio, i.e., a signal charge over pixel capacitance ratio, to reduce power consumption and maximize the signal-over-noise ratio (S/N). In this case, by assuming that the transistors have a dominating thermal noise, the following relation can be established [18]:

$$P \propto \left(\frac{Q}{C}\right)^{-m} \quad 2 \leq m \leq 4 \tag{3.1}$$

where parameter m characterizes the operational mode of the transistors, Q is the generated charge and P is the power. Therefore, by minimizing the pixel capacitance C, the power consumption can be reduced. In a simplified picture, a planar p-n junction capacitance can be treated like a parallel-plate capacitor ($C = A \cdot \frac{\epsilon\epsilon_0}{d}$). The extension of the space charge region d scales in this simplified geometry with $\sqrt{V_{tot}}$ the total voltage, defined by $V_{tot} = V_{ext} + V_{bi}$, where V_{ext} is the externally applied bias voltage and V_{bi} the built-in voltage [1] [19, p.299]. For the geometry of the ALPIDE chip, the extension of the depletion zone scales with $\sqrt[3]{V_{tot}}$, assuming it is spherically symmetric [20]. So by simply increasing the depletion volume, the capacitance decreases.

[1] The built-in voltage is the potential drop in a p-n junction in which no external voltage has been applied.

3.2. MAPS in ITS2: The ALPIDE Chips

MAPS have already been used at the RHIC accelerator for the STAR experiment [21]. The first implementation of MAPS at the ALICE experiment was the ALICE Pixel Detector (ALPIDE) which is currently in use for the ITS2. Figure 10 shows a schematic overview of the cross-section for a pixel of the ALPIDE chip using the so-called standard process for charge collection.

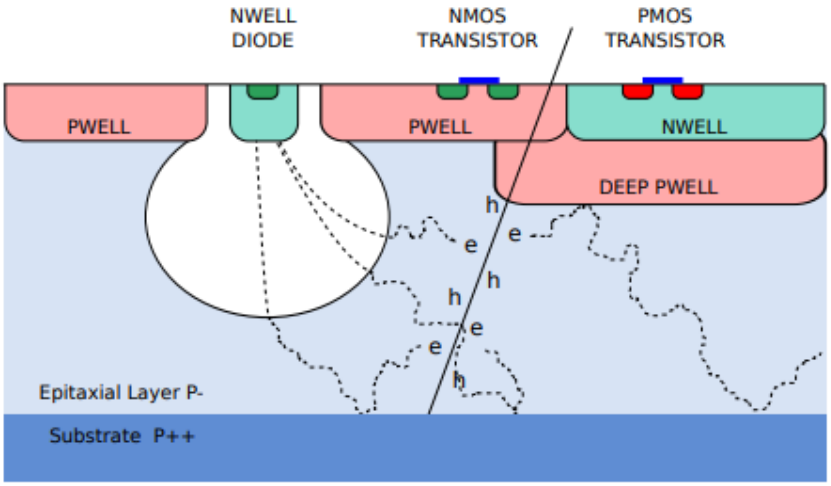


Figure 10 Sketch of the doping layout for the MAPS used for ALPIDE. The process of charge collection of the particle is also shown (so-called standard process) [22, p.12]

The transistor feature size, indicated by NMOS and PMOS on the surface, is $180\,\mathrm{nm}$ and based on the TowerJazz CMOS Imaging Process technology [22]. A charged particle passes through the silicon and loses energy via electromagnetic scattering with the electrons inside the material, creating electron-hole pairs. The epitaxial layer and the n-well diode serve the p and n part of the junction, respectively. The deep p-well serves the purpose of shielding the circuitry from the rest of the active layer. The combination of PMOS and NMOS transistors indicates the CMOS circuitry implanted on the surface of the detector. The substrate provides an electrical contact and a structural foundation. Electron-hole pairs diffuse inside the epitaxial layer until they reach the depletion zone, marked in white in Figure 10, and then start drifting towards the collection diode [18]. The back bias voltages get applied between the substrate and the n-well diode. With this architecture, prototypes of the ALPIDE chip, namely pALPIDE-1, pALPIDE-2, and pALPIDE-3, have demonstrated a detection efficiency more than 99% even in the presence of irradiation damage ([6], [23], [7, p.73], [24]).

A schematic sketch of the in-pixel circuitry for the ALPIDE chip is shown in Figure 11. The signal created inside the pixel passes through the collection diode. The input stage is equipped with a reset mechanism. Figure 11 demonstrates a setup when the system gets reset via a diode [25, p.87]. In this case, a reset voltage is applied to the chip to restore the baseline. A small capacitor is also located inside the input stage for injecting test charges inside the

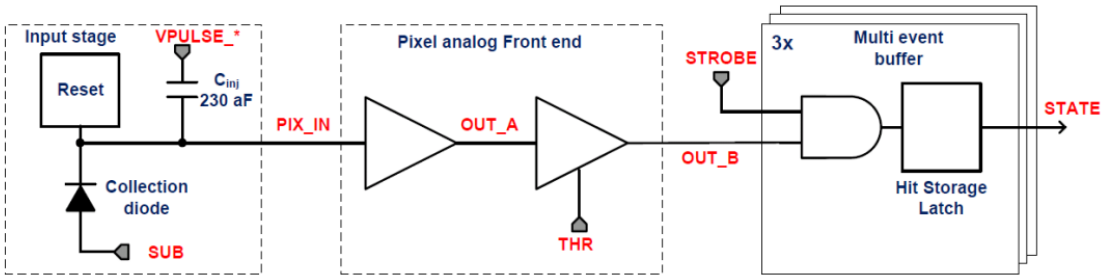


Figure 11 Block schematic of the ALPIDE in-pixel circuitry [7, p.59]

circuitry for test and calibration purposes. By fine-tuning the VPULSE, electronic properties such as the readout threshold can be tested. The output signal PIX_IN then gets amplified, and a threshold THR gets applied via a comparator inside the pixel analog Front end. The amplified output OUT_B then latches inside a multi-event buffer [7, p.58-61]. The readout is carried out with the help of a priority encoder [26]. The system can be run in continuous mode and triggered mode [27]. The final ALPIDE chip allows for a spatial resolution of up to $5\,\mu m$. It maintains high performance even when exposed to irradiation levels ranging up to 500 krad and an integrated particle fluence[2] of $10^{13}1\,\mathrm{MeV n_{eq}/cm^2}$ [7, p.79]. The ALPIDE chip fulfills the requirements to be implemented in the ITS2. However, the read-out and the pixel technology can be further optimized. Simulations have been performed to characterize the doping profile of the standard process [20]. These show that the epitaxial layer is not fully depleted and has a spherical-shaped depletion geometry. In order to increase the depletion volume, a highly resistive and thick epitaxial layer has to be utilized, which results in reduced charge sharing and improved charge collection time.

3.3. Modified Process: Improvements in the layout

One way of achieving full depletion of the epitaxial layer is by inserting a low-dose n-type implant inside the active layer. Figure 12 shows the modified process (left panel) and the

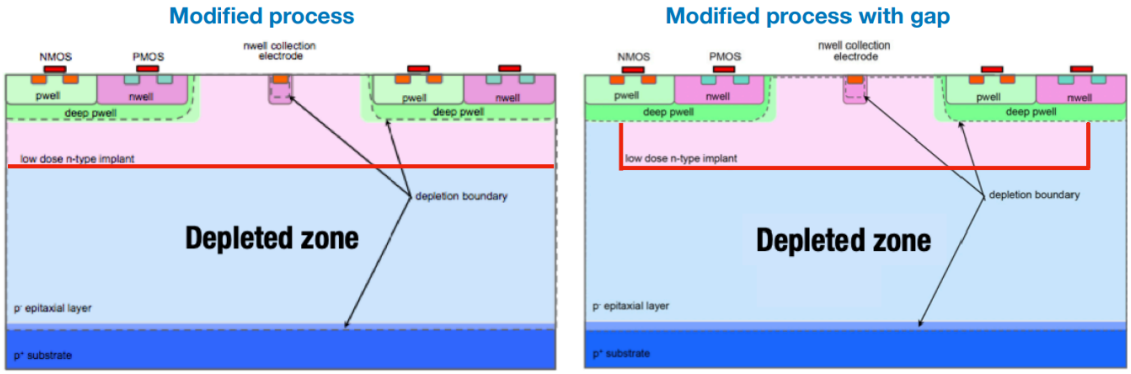


Figure 12 Schematic cross-section of one pixel for the modified process (left panel) and modified process with a gap (right panel) [28]

[2] Fluence is the time-integrated flux of radioactive particles

modified process with a gap between each pixel. By implementing this n-type layer, the junction turns into a planar junction, thus creating a depletion layer, which in theory, fills up most of the epitaxial layer. One feature of this implantation is that the signal rise time depends less on the position of the interaction and exhibits a shorter charge collection duration than the standard process ([29], [20]). A higher radiation tolerance was also observed for the modified process. Also, charge sharing is significantly reduced between adjacent pixels, which was already quantified with ^{55}Fe source measurements. Yet, simulations have shown that the total electric field of the modified process is zero in the corners (Figure 12 top right and left in the epitaxial layer). The area of this region decreases with the pitch size [3] of the pixel getting smaller [30]. In this case, by decreasing the pitch size, higher detection efficiencies for the modified process have been observed in simulations [20]. This effect can significantly reduce detection efficiencies at higher radiation exposure. Implanting a gap between each pixel, shown on the right panel of Figure 12, creates a higher lateral electric field, thus reducing charge sharing even more. The efficiencies can be optimal even for higher threshold settings and pitch sizes (predicted by simulations) [20]. The modified process with a gap also exhibits faster collection times ([30],[31]). Additionally, it also has been observed that signal fall times are more uniform for different signal amplitudes for the modified process with a gap ([29],[20], [32]).

[3] Pitch size is the lateral extension of each pixel

4. The Analogue Pixel Testing System (APTS)

As mentioned before, the chips are available in multiple doping profiles and pitch sizes. To characterize properties such as charge collection efficiency, detection efficiency, radiation hardness, and charge collection time, different test structure have been created.

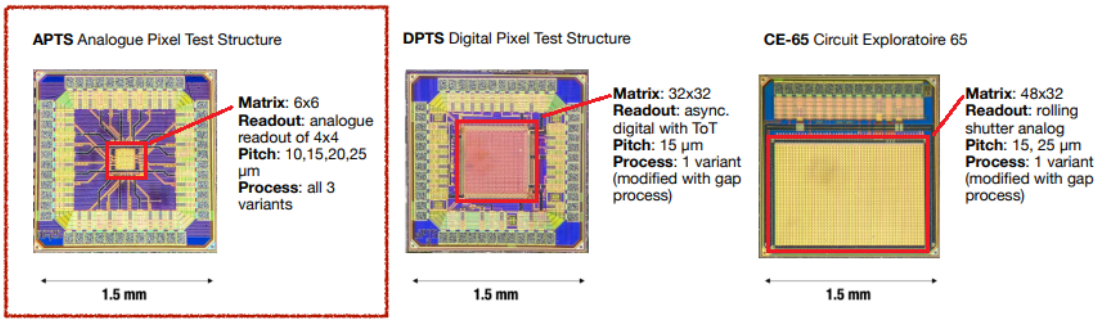


Figure 13 The Analog Pixel Testing Structure (On the left) and Digital Pixel Testing Structure (Middle) and the Circuit Exploratoire 65 (On the right). The pixel matrix is marked in red [28]

The APTS, DPTS, and CE-65 chips are shown in Figure 13. The APTS chip has outer dimensions of $1.5\,\mathrm{mm}$ by $1.5\,\mathrm{mm}$. All three doping profiles with a pixel pitch size of $10\,\mu\mathrm{m}$, $15\,\mu\mathrm{m}$, $20\,\mu\mathrm{m}$, and $25\,\mu\mathrm{m}$ have been manufactured for this test structure. At the innermost center, the pixels are located and marked in red. In Figure 13, a 6×6 matrix with only a 4×4 active matrix is shown. The edge pixels are only there to eliminate edge effects. The DPTS in the center is characterized by a 32×32 pixel matrix and digital readout with a time over the threshold (ToT) decoder. Only a 15-pitch size with the modified process with a gap has been studied for the DPTS chip. A threshold and time over the threshold study have already been conducted for the DPTS for varying bias settings. Also, test beam analysis and measurements with a ^{55}Fe in the laboratory have been carried out [33]. Another test structure is the CE-65 (Circuit Exploratoire 65) with a rolling shutter readout shown on the right panel of Figure 13. The matrix is 48×32 pixels, the pitch sizes are 15 and 25, and only the modified process with a gap is being studied [34]. In the framework of this thesis, we have investigated the different versions of the APTS chips.

4.1. Overview on the different versions of the APTS

The Analog Pixel Test Structure (APTS) is available in different configurations. The output buffer types are either the Source Follower (SF) version, which is in use for this thesis, or an Operational Amplifier (OPMAP[1]) version [34]. The in-pixel amplifier can be AC or DC coupled for the SF type. Also, multiplexed chips containing four sub-matrices have been produced with the readout happening the same way as for the APTS SF variant [36].

[1] Operational Amplifiers are high gain dc-coupled differential amplifiers with a single-ended output [35, p.176]

4.2. Principle of operation

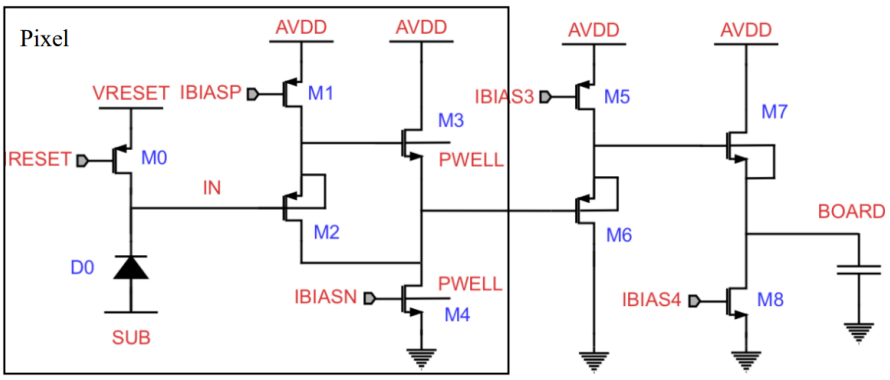


Figure 14 Schematic block diagram of the APTS source follower chip [36]

Figure 14 shows a schematic overview of the APTS source follower with DC coupling [36]. The signal comes from the collection diode D0. After the voltage has dropped to a certain extent, the PMOS transistor (M0) turns on, allowing current to flow from the drain to the source discharging the collection electrode. The voltage gets set to a reference level called reset voltage (VRESET). Resetting the potential to VRESET is essential to ensure that the transistor remains within the optimal working conditions. The reset current IRESET defines the time scale at which the collection diode resets to baseline. The DC voltages on the collection electrode closely resemble the voltages set at the source of M0, VRESET, in this case. The substrate (PSUB), as well as the bulk of the NMOS transistors (PWELL) in each pixel, is biased with a negative bias voltage, referred to as back bias voltage V_{bb}. Two source follower stages are integrated via PMOS (M1 and M2) and NMOS (M3 and M4) transistors inside the pixel. Transistors M1 and M4 provide biasing of the currents, IBIASP and IBIASN, respectively. The output from the n-type follower stage is directly linked to the drain of the input transistor of the initial stage. This connection enables the input transistor in the readout chain to replicate the voltage signal from the collection electrode in both the source and the drain. An additional pair of source-follower stages (M5, M6 and M7, M8), controlled by IBIAS3 and IBIAS4, connect the matrix outputs with the analog output pads. By using a source follower circuit, the capacitive load on the collection diode is minimized. In general, the purpose of the source follower is to convert the input voltage at the gate to an output current (drain current) of a transistor. In these cases, a high input impedance gets transformed into a much lower output impedance governed by the transconductance ($g_m = \frac{i_{out}}{v_{in}}$) of the field effective transistor [35, p.130-135]. The gain ($G = \frac{v_{out}}{v_{in}}$) at each source follower should be roughly one[2]. The proper biasing of each parameter (IBIASP, IBIASN, ...) was already established, aiming for optimal performance. The main goal was a constant gain for the signals before and after the source follower stages. In this case, the total linearity between VRESET and the baseline for the signal after the amplification has been studied [37]. Due to the analog nature of this circuitry, the output signal of the pixel can be directly measured with an oscilloscope allowing for the study of signal waveforms.

[2] Slightly smaller than one

5. Charactarization of the APTS Chips

5.1. Radioactive Sources

Ideal test conditions for the pixel response could be achieved by using a constant charge injected into a small volume of the active pixel. Therefore, well-known sources with definite energy peaks have been utilized. For this reason, the ^{55}Fe source [1] is an excellent choice, and it has been used for sensor optimization for the ITS2 and ITS3 ([31], [7, p.34-36], [32],[33], [20], [38], ...). The isotope ^{55}Fe decays into ^{55}Mn through electron capture:

$$^{55}_{26}\text{Fe} + e^- \rightarrow ^{55}_{25}\text{ Mn} + \nu_e. \tag{5.1}$$

The vacancy in the K-Shell then gets filled by an electron from the outer shells. This process results in the emission of an X-ray photon with an energy of $K_\alpha = 5.9\,\text{keV}$ or with $K_\beta = 6.5\,\text{keV}$ [39]. The X-ray photon then interacts with the silicon inside the detector through the photoelectric effect [19, p.77], creating electron-hole pairs in the substrate. It is assumed that the photon deposits all of its energy inside the material of the detector. The average energy needed to create an electron-hole pair in silicon is $E_{e-h} = 3.6\,\text{eV}$ [40, p. 79], resulting in roughly 1640 and 1800 electrons for the K_α and K_β photon, respectively. With a precise knowledge of the total energy deposited in the material, the chip's charge collection properties and efficiency can be studied. The usage of ^{55}Fe also allows for comparing different doping layouts, pitch sizes, and back bias voltages. Additionally, the energy deposited by the K_α or K_β photon is larger than the one expected for Minimum Ionizing Particles (MIPs). In this case, the energy loss per unit of length is $60\,\text{eV}/\mu\text{m}$ for a $20\,\mu\text{m}$ to $30\,\mu\text{m}$ thick sensitive layer resulting in $1.2\,\text{keV}$ total energy deposited for a $20\,\mu\text{m}$ thickness [7, p.25].
In addition to the introduced iron source, a relatively low energy source is required to calibrate the linearity of the detector response with respect to the deposited energy in the material. Similar to iron, ^{41}Ca also undergoes a K-shell capture:

$$^{41}_{20}\text{Ca} + e^- \rightarrow ^{41}_{19}\text{ K} + \nu_e, \tag{5.2}$$

which results in monoenergetic $K_\alpha = 3.3\,\text{keV}$ and $K_\beta = 3.59\,\text{keV}$ x-Ray beams [41], creating about 917 and 997 electrons in the detector medium, respectively. A linear relation will be expected between the signal and the deposited energy in the medium. One part of this thesis was to verify if that linearity is perfectly implemented in the amplifier design.

[1] A list of the radioactive sources at TUM is shown in the Appendix

5.2. The Setup

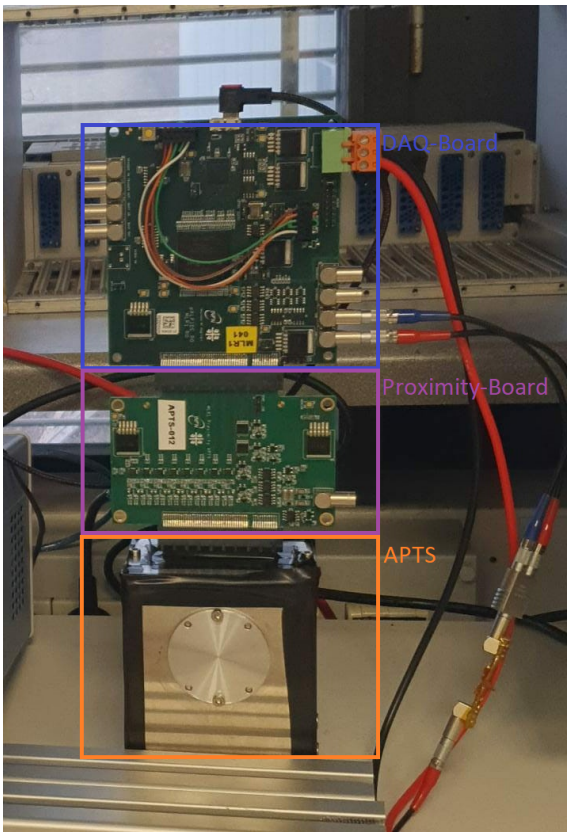


Figure 15 The experimental setup: At the bottom part of the picture, the detector box housing the APTS chip is shown (orange). It connects to a Proximity Board is responsible for supplying voltages (purple). On the top is the DAQ-Board responsible for converting the signals into computer-readable signals as well as communication between chip and PC

The experimental setup for the characterization of the APTS chips at TUM is shown in Figure 15. The APTS chip is kept inside an aluminum box. To minimize the noise from electromagnetic radiation coming from outside, as well as to protect the chip from external impacts such as accidental mechanical contact. The box also provides an opening where the radioactive sources can be placed via a specialized source holder. The schematics of the APTS chip with the source are shown in Figure 16.

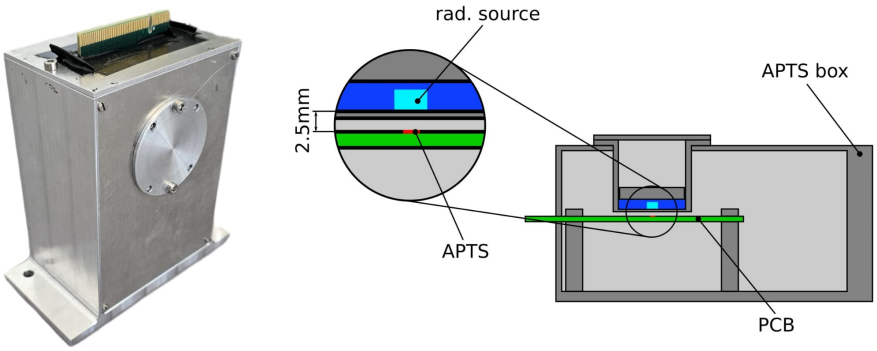


Figure 16 Schematic figure of the aluminum Box. The Source is kept inside a cylindrical source holder roughly $2.5\,\mathrm{mm}$ away from the chip mechanically mounted via screws

The box provides mechanical support for the radioactive source and chip while minimizing the distance between these two. The source can be placed at the closest of about $2.5\,\mathrm{mm}$ to the chip, which can vary on the source holder geometry. The proximity board is situated right above the aluminum box, indicated by a purple frame in Figure 15. The board provides the necessary voltages and currents for the chip as well as converting the analog signals into digital via an Analog Digital Converter (ADC). Right above the proximity board, the DAQ board is located, illustrated with a blue frame in Figure 15. This board hosts an FPGA, allows to connect bias voltage, and enables the readout and communication between the computer and APTS via USB.

5.3. Experimental results

The chips analyzed in this work are presented in the following list:

APTS	AF10P_W22B25	AF15P_W22B19	AF20P_W22B53	AF25P_W22B53
Fe^{55}	0.0 , 1.2 , 2.4 , 3.6 , 4.8			
Ca^{41}	/	/	2.4 , 4.8	2.4

Table 2 An overview of which chips have been used for each measurement. The chips are listed on the first row, and each entry of the table corresponds to the applied back bias voltage in the units of volt

Pitch sizes varying from $10\,\mu\mathrm{m}$ to $25\,\mu\mathrm{m}$ were used and indicated in the name as the third and fourth characters. Chips with a doping profile following the modified process with a gap have been tested exclusively (cf. section 3.3). Note that for the Calcium source, only two chips were investigated. Due to the limited time available for the open calcium source and the low source activity inside the source holder.

5.3.1. Gain calibration

Before performing any measurement, a gain calibration between VRESET and the baseline signal has to be carried out, as introduced in chapter 4.2. Figure 17 shows an example of these gain calibration curves. Each line corresponds to a pixel inside the APTS (16 in total). On the left panel, the reset voltage V_{Reset} is plotted against the baseline voltage after the amplification inside the analog front end. V_{Reset} is the voltage the pixel gets restored to after the n-well diode has finished collecting the generated charge by the incident particle, which drops the voltage inside the pixel. The gain is roughly 0.65, which is a result of the multiple source follower stages, which have a gain smaller than one each. On the right panel, the derivative of the Baseline-V_RESET curve is shown. The linearity in the Baseline - V_RESET curves leads to two significant consequences. Firstly, after converting the analog signal into digital via an ADC, the total voltage drop inside the pixel right before the first source follower can be easily calculated. Secondly, this plot verifies the functionality of the analog front-end

amplification and ensures that the signal range falls within its linear operating range.

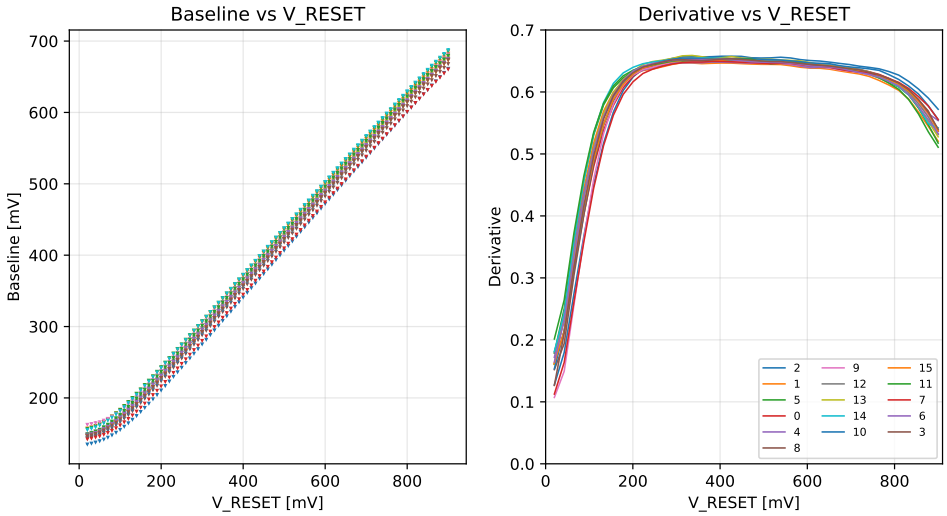


Figure 17 Gain Calibration for the 20 Pitch Chip with $V_{bb} = -2.4\,\mathrm{V}$. Left panel: Reset voltage V_RESET plotted against the Baseline voltage after amplification. Right panel: Derivative of the Baseline vs. Reset voltage. Each line corresponds to a pixel of the APTS

5.3.2. The ^{55}Fe Measurement

In this section, the effect of different pitch sizes and back bias voltages on the APTS chip are investigated using the ^{55}Fe source.

5.3.2.1 Analysis of Matrix vs. Seed signal and charge collection efficiency (CCE)

Before discussing the matrix signal and the charge collection efficiency (CCE), the seed signal [2] distribution for different numbers of pixels fired, called cluster size, is investigated. Figure 18 shows the seed signal distribution for the 20-pitch-sized chip with back bias voltage $V_{bb} = -4.8\,\mathrm{V}$. A large threshold of $20\,\mathrm{mV}$ is applied since the pixel's thermal and electrical noise can significantly affect the cluster size distribution [3].

In Figure 18, the seed signal distribution is split into different cluster sizes. Histograms for the seed signal for all cluster sizes (top left), cluster size one (top right), cluster size two (bottom left), and cluster size bigger than two (bottom right) are shown. The two distinct peaks of the iron source are clearly visible and indicated by the cluster size = 1 that all the generated charge generated by the X-ray photon of the ^{55}Fe has been collected by only one pixel. Also, a continuous tail is present down to $20\,\mathrm{mV}$. The main contribution of the tail is the cluster size of two, which indicates charge sharing dominantly occurs between adjacent pixels. The remaining part, corresponding to cluster size ≥ 3, is negligible. This result shows that the modified process with a gap between pixels minimizes charge sharing.

[2] The seed signal is the signal of the pixel showing the largest amplitude in that event
[3] This will be further discussed in section 5.3.5

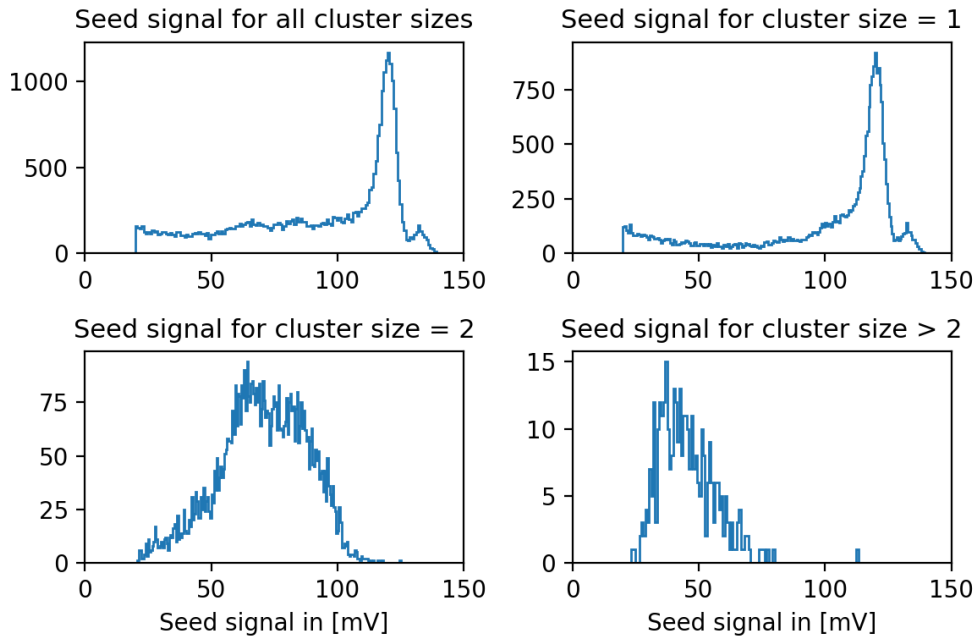


Figure 18 Histograms of the seed signal distribution divided for different cluster sizes at -4.8 V back bias for the 20-pitch chip: Top left panel shows events for all cluster sizes. The top right panel illustrates only cluster size = 1 events. On the bottom left panel, the cluster size = 2 events, and on the bottom right, the cluster size > 2 events are displayed.

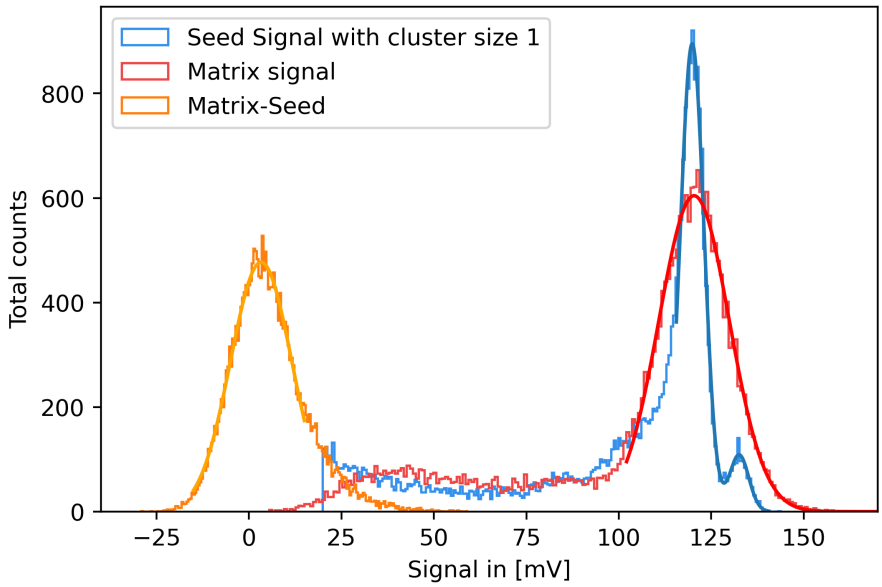


Figure 19 Seed signal of cluster size 1 vs. Matrix signal vs. The difference between matrix and seed (Seed-Matrix) for the 20 pitch-size chip at -4.8 V back bias voltage

Figure 19 shows the matrix signal (red), the seed signal of cluster size one (blue), and the difference between these two signals (yellow) for the four central pixels. The matrix signal is the sum of the 3x3 pixel matrix surrounding the seed pixel. A double Gaussian function was fitted for the seed signal and a single Gaussian for the matrix and (matrix-seed) signal. The width of the Gaussian peak for the matrix signal is $\sqrt{9}$-times bigger than the width of the

K_α Peak in the seed signal spectrum. This is expected since the noise of the surrounding pixels is added. Nine pixels contribute to one matrix signal; correspondingly, the standard deviation increases $\sqrt{9}$ times. Figure 20 shows the correlation between the seed signals with cluster size 1 and the corresponding matrix signal. For the lower range, the slope of the correlation is almost one; for reference, a dashed line with $x = y$ is displayed. But when approaching the signal range in which the K_α and K_β peaks are located, the correlation slope increases drastically. As another reference, the function $y = 4 \cdot x + b$ going through the point ($\text{Signal}_{\text{seed}} = 120\,\text{mV}$, $\text{Signal}_{\text{matrix}} = 120\,\text{mV}$) is shown in Figure 20. In this case, for smaller variations of the seed signals, much more significant variations of the matrix signals can be observed. This can be mainly attributed to the addition of correlated noise to all pixels in the matrix signal, which causes the signal to be more spread out.

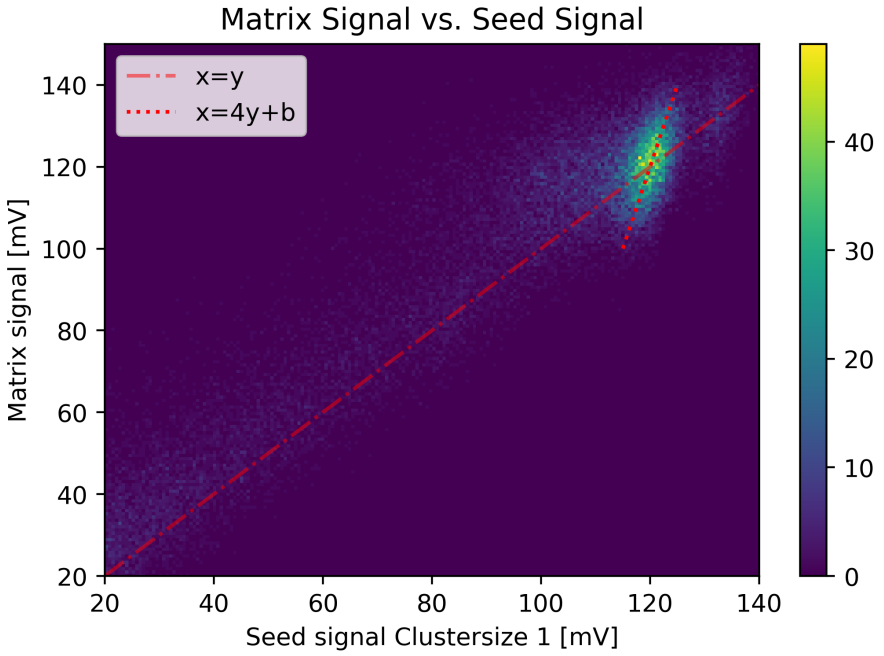


Figure 20 Matrix Signal vs. Seed signal for the 20 Pitch chip at $V_{bb} = -4.8\,\text{V}$. The dashed lines are used as a reference

When the seed signal gets subtracted from the matrix signal, only a peak should remain. The remaining signal is, in this case, slightly shifted ($\mu = 3.07 \pm 0.09$), and the width of the fitted Gaussian is as expected $\sqrt{8}$ times bigger than the seed signal width.

A way of quantifying the charge collection efficiency is by comparing the seed and matrix signals of the whole pixel. The ratio of the seed signal of cluster size = 1, and the matrix signal defines the charge collection efficiency (CCE):

$$\text{CCE} = \frac{V_{seed}}{V_{matrix}}. \tag{5.3}$$

Due to the broader distribution of the matrix signal, the K_β line cannot be resolved. For this reason, to calculate the charge collection efficiency, a cut for the matrix signal has been made;

see Figure 21. Without a cut, a charge collection efficiency of over 100% has been observed. Only events within a 1 sigma range for the K_α peak in the seed signal have been used. Due to relatively low statistics on the K_β peak, only the K_α peak was used to calculate the charge collection efficiency. Figure 21 shows the deviation of the mean value for the cut (blue) and uncut (yellow) matrix signal distributions. The corresponding seed signals are shown with a green color. With the mean value of the cut matrix signal, a charge collection efficiency of

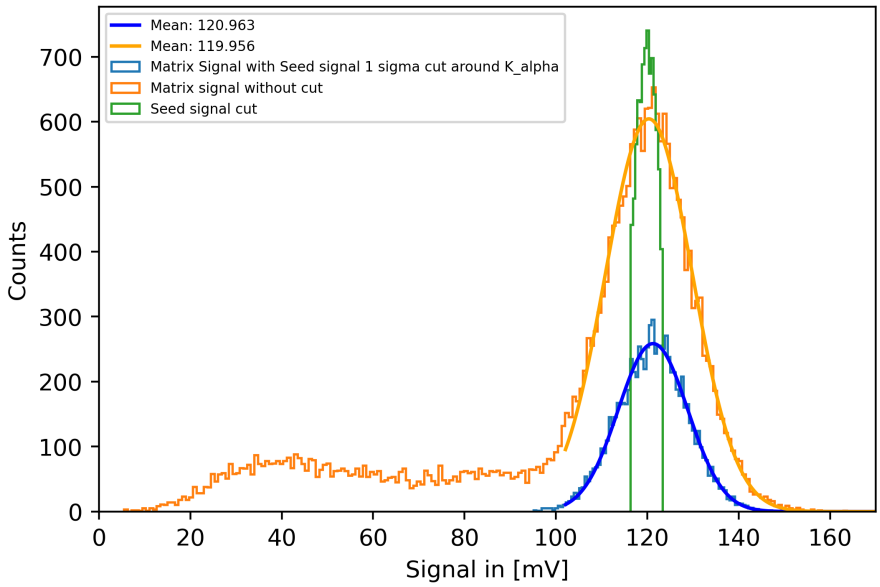


Figure 21 Comparison between the uncut matrix signal and the matrix signal only corresponding to seed signal events 1 σ around the K_α

CCE$= 98.8 \pm 0.1\%$ has been calculated.

5.3.2.2 APTS spectra for different V_{bb}

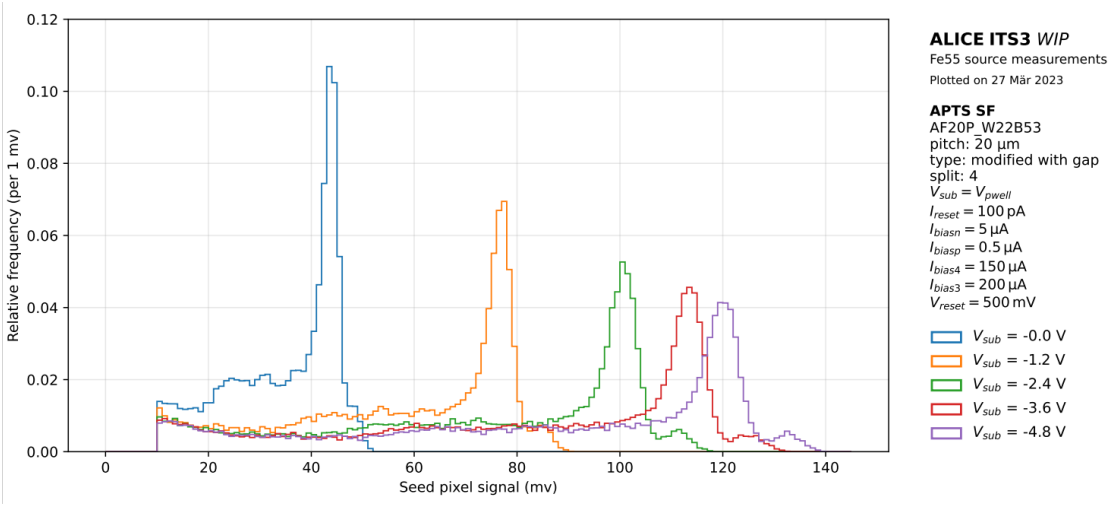
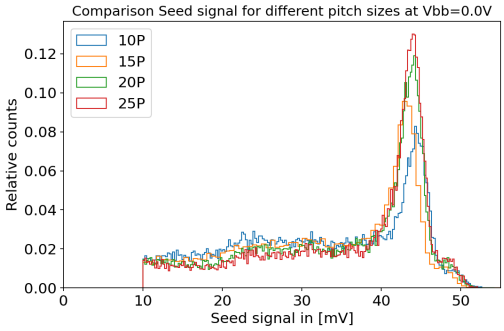


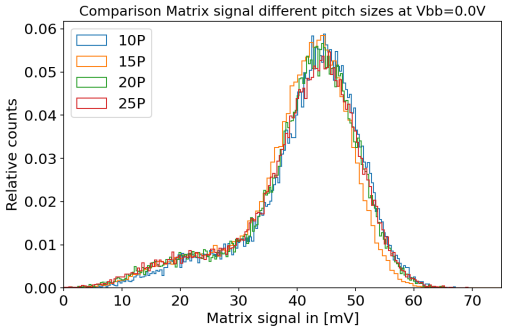
Figure 22 Comparison of different back bias voltages for the 20-pitch size chip. The seed signal of the four central pixels was taken

Figure 22 shows the iron seed signal spectrum for different back bias voltages for the pitch $20\,\mu m$ sized pixel. The data for this histogram was taken from the four innermost pixels of the detector. On the right-hand side of the Figure, all voltages and currents required for operating the silicon detector are listed (cf. section 4.2). Increasing the back bias voltage on the substrate causes an increased seed signal as can be seen from the shift of the characteristic ^{55}Fe peaks of the histograms. This means that changing the back bias voltage changes the detector capacitance. Increasing the bias voltage decreases the total capacitance, increasing $V_{out} = Q/C_{pix}$, the output voltage of each pixel. In this case, Q should be constant (assuming the photon creates the same charge for each event), and C_{pix} should decrease, thus increasing the output voltage.

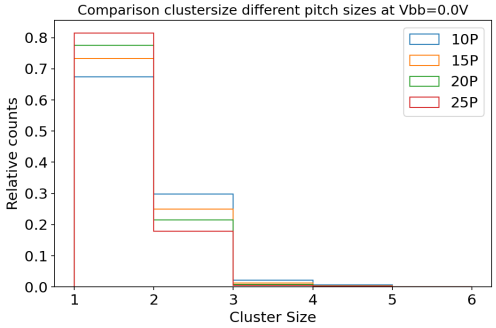
5.3.2.3 Comparison between different pixel sizes



(a) Comparison of different pitch sizes of the seed pixel signal with a threshold at $10\,mV$ ($V_{bb} = 0.0$ V)



(b) Comparison of different pitch sizes of the matrix signal ($V_{bb} = 0.0$ V)

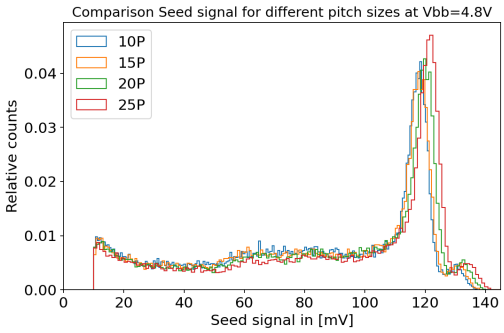


(c) Comparison of different pitch sizes of the cluster size distribution with a threshold at 300 electrons ($V_{bb} = 0.0$ V)

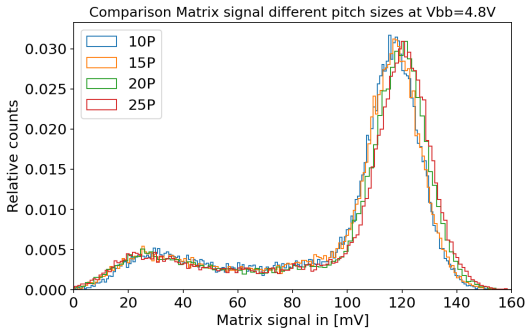
Figure 23 Comparison of the different pitch sizes a) Seed signal b) Matrix Signals c) Cluster sizes for back bias 0.0 V

Following the spectrum analysis for one chip, different chips of various pitch sizes are compared in this section. In Figure 23, the seed signal distribution (panel a), matrix signal distribution (panel b), and cluster size distribution (panel c) for an applied back bias voltage of $0.0\,V$ are shown. A $10\,mV$ threshold for the seed signal has been applied. In order to compare the cluster size distribution, a threshold of 300 electrons has been performed separately. The threshold value in milli-volts has been calculated with $\text{Thr}_{mv} = \text{Thr}_{e^-} \cdot \frac{V_{K_\alpha}}{1640}$.
V_{K_α} is the mean value of the K_α photons, and 1640 correspond to the energy of the K_α-peak

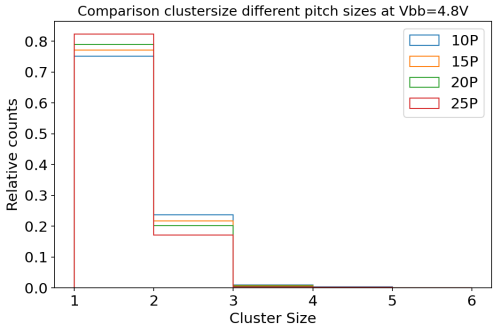
converted in electrons and Thr_{mv}, Thr_{e^-} are the threshold values in milli-volts and electrons respectively. Note that the threshold scales with the mean value of the seed signal for the K_α peak. The chip with the pitch size of $25\,\mu\text{m}$ has the most significant contribution of cluster size one, which decreases for smaller pitch sizes. The peaks of the seed signal nearly overlap, but the $10\,\mu\text{m}$ and $15\,\mu\text{m}$ pitch chips are slightly shifted. However, the matrix signal distribution for all pitch sizes seems to be more uniform; see Figure 23 panel b. The higher contribution of cluster size one events is due to the geometry of a larger pixel surface area. For geometrical reasons, it is less probable for the secondary electrons to cross the pixel border.



(a) Comparison of different pitch sizes of the seed pixel signal with a threshold at $10\,\text{mV}$ ($V_{bb} = -4.8\,\text{V}$)



(b) Comparison of different pitch sizes of the matrix signal ($V_{bb} = -4.8\,\text{V}$)



(c) Comparison of different pitch sizes of the cluster size distribution with a threshold at 300 electrons ($V_{bb} = -4.8\,\text{V}$)

Figure 24 Comparison of the different pitch sizes a) Seed signal b) Matrix signal c) Cluster sizes for back bias -4.8 V

After increasing the back bias voltage (Figure 24), the relative contribution of cluster size one events for all pitch sizes increases. For example, the cluster size one events for the 10 pitch pixel increase from about 0.68% to 0.75%; see Figure 23c and Figure 24c. Figure 24a shows a clear tendency for higher signals as the pitch size increases. The main K_α peak for the $25\,\mu\text{m}$ (red curve) is higher than the other chips, indicating an increase in cluster size one events. The matrix signal of the 25 Pitch chip is shifted to the right as well.

Figure 25 shows the charge collection efficiency (top left), the calculated capacitance (top right), the mean cluster size (bottom left), and the seed signal for the K_α peak on the bottom right plotted against different back bias voltages. The charge collection efficiency is close to 100% and exhibits an increase for bigger back bias voltages. With the seed signal distribution

of cluster size = 1, the capacitance of the pixel detector can be calculated with:

$$C = \frac{N_{e^-} \cdot e}{V_{Seed,K_\alpha}}, \tag{5.4}$$

where N_{e^-} is the amount of electron generated by the Iron K_α photon (roughly 1640), e the electric charge constant, and V_{Seed,K_α} the seed signal for the peak. For example, for the 20 Pitch at $V_{bb} = -4.8\,\text{V}$ the capacitance has been calculated to be $C = 2.20 \pm 0.01\text{fF}$. The Capacitance decreases for higher back bias voltages. As discussed in Section 5.3.2.2, the depletion zone of the chip increases with increasing V_{bb}, therefore, reducing the pixel capacitance. It is also visible that the capacitance saturates for higher back bias voltages, indicating that the substrate is almost fully depleted and cannot increase anymore.
The capacitance, as well as the seed signal, does not change significantly for different pitch sizes. But a clear trend is seen between the pitch sizes for the mean cluster sizes. In addition, the mean cluster size decreases for higher bias voltages, and it is evident that bigger pitch sizes also minimize the mean cluster size. These results are consistent with the increase in the charge collection efficiency. In this case, the highest charge collection efficiency is established by the $25\,\mu\text{m}$ chip and increases for higher back bias voltages. Corresponding to that, the mean cluster size is also the lowest and decreases slightly for higher back bias voltages.

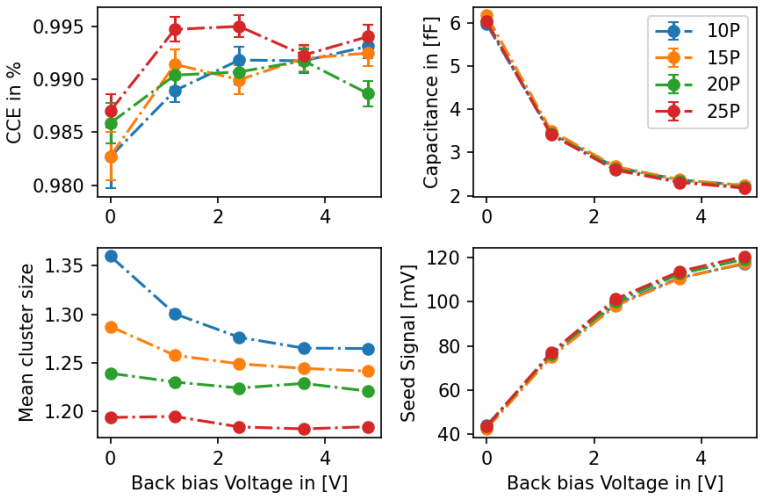


Figure 25 Summary of comparison between all pitch sizes: Top left charge collection efficiency; Top right Capacitance; Bottom left mean cluster size; Bottom right K_α peak of the seed signal

5.3.3. ^{41}Ca Measurement

Measurements with the radioactive ^{41}Ca source will be presented in this section. As mentioned in section 5.1, the ^{41}Ca source provides an X-ray photon peak with a lower seed signal, optimal to study the linearity and offset of the calibration of the signal as a function of deposited energy. The K_α and K_β gammas of ^{55}Fe are insufficient in this study since these two energies are quite close.

The Calcium source has a relatively low activity, so the signal-to-noise ratio is expected to be larger than in the ^{55}Fe measurement for a given threshold. Only the seed signal of the four central pixels were used for the energy calibration.

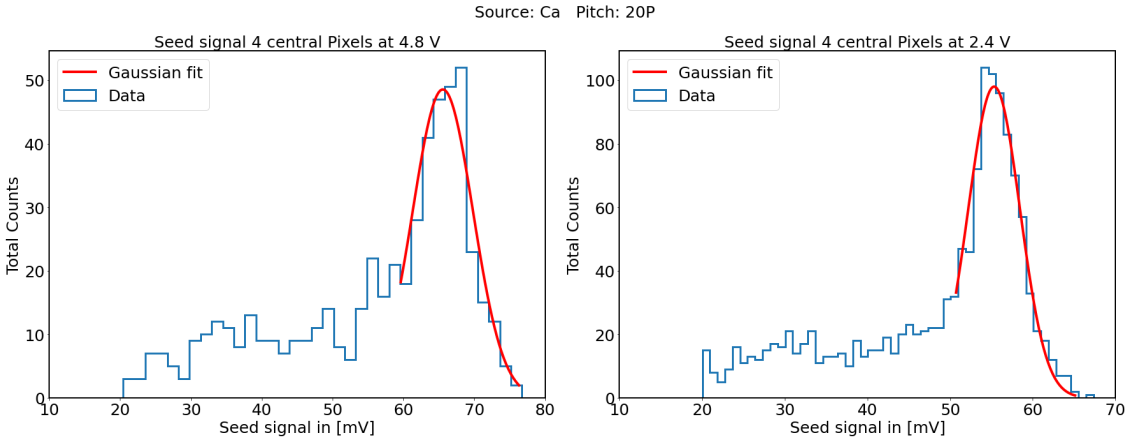


Figure 26 Seed signal spectrum of ^{41}Ca for the 20 pitch size chip: Right $V_{Vbb} = -2.4\,\mathrm{V}$; Left $V_{Vbb} = -4.8\,\mathrm{V}$

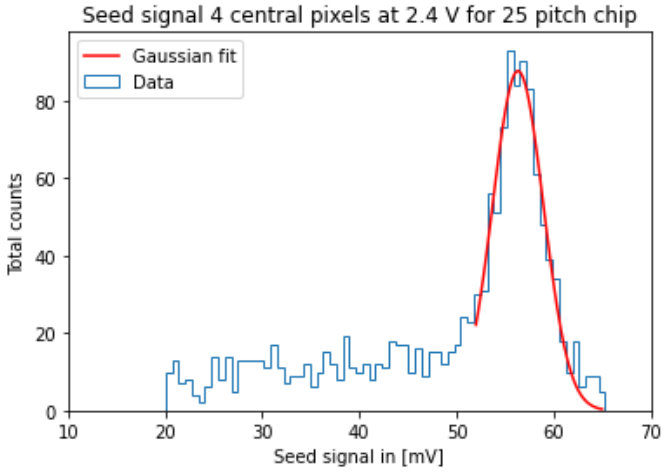
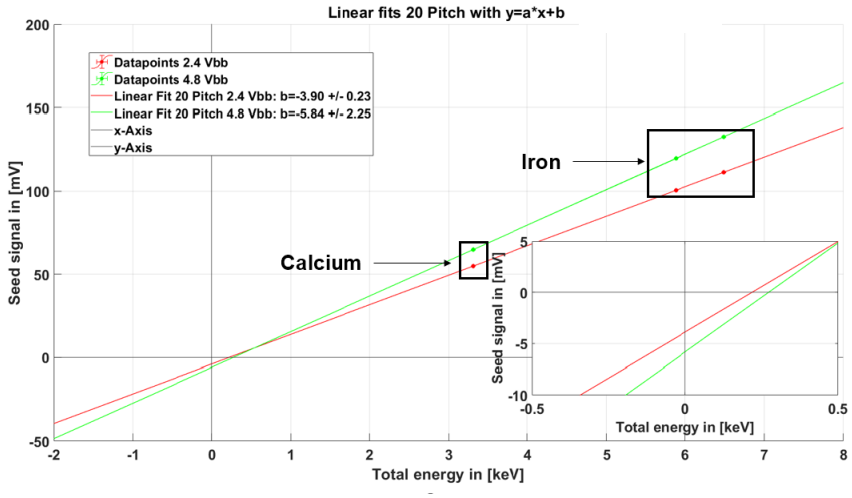


Figure 27 Seed signal spectrum of ^{41}Ca for the 25 pitch size chip. Signal amplitudes below $20\,\mathrm{mV}$ are cut by the analysis software

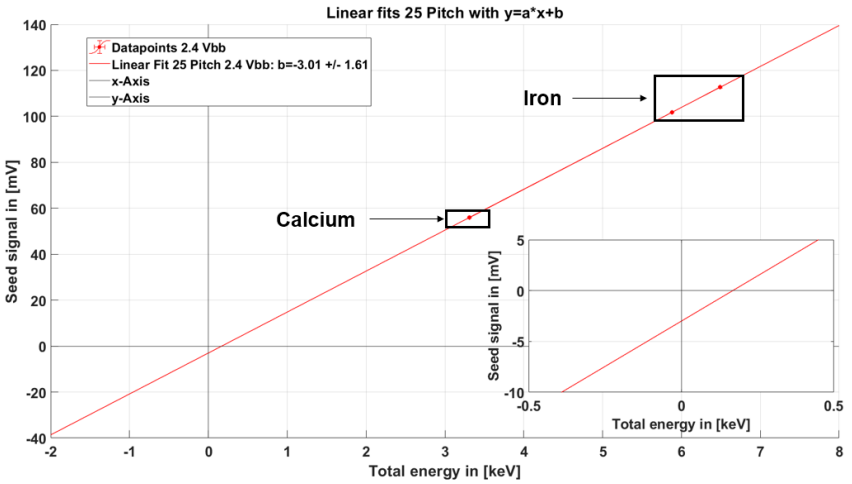
Figure 26 and 27 show the spectra of ^{41}Ca for the 20-pitch and 25-pitch sized chip, respectively. Note that, for the 20-pitch chip at $-4.8\,\mathrm{V}$ back bias, the measurement duration was shorter than the rest, resulting in half as many counts as for the other measurements. Due to this reason, the bin size for this dataset (Figure 26 left) is increased. Using the mean value of

the seed signal peak obtained in the ^{41}Ca measurement, in combination with the Iron peaks, the deposited energy in the material can be calibrated against the seed signal. As expected, an increase in the back bias voltage increases the seed signal as well; see Figure 26. In this case, the mean peak changed from $\mu_{20P;2.4} = 54.87 \pm 0.02$ mV to $\mu_{20P;4.8} = 64.79 \pm 0.13$ mV. And for the 25 Pitch chip, the mean is centered around $\mu_{25P,2.4} = 56.00 \pm 0.01$ mV.

5.3.4. Energy calibration



(a) Energy calibration: Seed signal vs. total deposited energy for the 20-pitch sensor. The red line is for $V_{bb} = -2.4$ V and green curve is for $V_{bb} = -4.8$ V. Linear offset is indicated by parameter b



(b) Energy calibration: Seed signal vs. total deposited energy for the 25-pitch sensor at a back bias of 2.4 V. Linear offset is indicated by parameter b

Figure 28 Energy calibration for a) 20 Pitch size b) 25 Pitch size chip. Data points, as well as a linear fit, are shown. The zoom of the origin is also shown in the bottom right corner of each plot, indicating that all linear fits do not cross absolute zero.

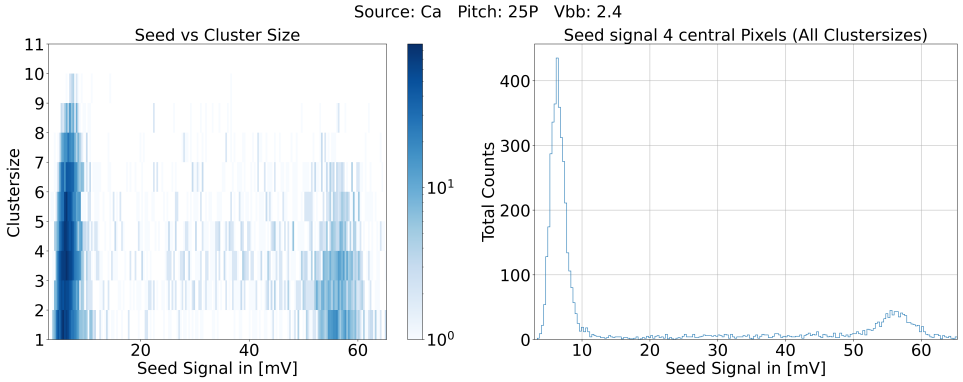
Figure 28 shows the energy calibrations. In Figure 28a, the calibration of the 20-pitch chip is shown. On the bottom of Figure 28b, the 25-pitch chip is shown. The offset parameter b from the linear fit function $y = a \cdot x + b$ is displayed. The data points of calcium and iron measurements are also indicated. ^{41}Ca creates $K_\alpha = 3.31$ keV and $K_\beta = 3.59$ keV photons,

which cannot be resolved in this case [41]. Therefore an average energy of $\bar{E} = 3.33\,\mathrm{keV}$ has been used. A zoom around the origin of the coordinate system is shown for each plot on the bottom right.

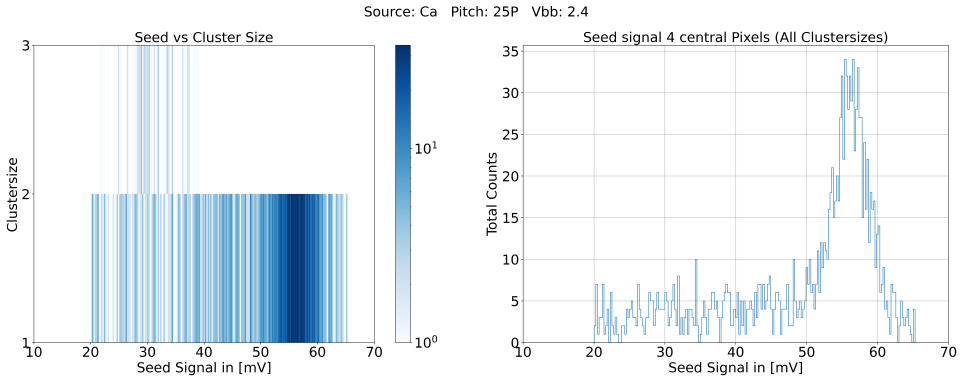
For all bias settings and pitch sizes, the linear graph crosses the y-axis at small negative values. Whereas a positive offset was observed for the remaining signal when subtracting the seed signal from the matrix signal (cf. Section 5.3.2). A negative offset means that not all energy depositions can be detected with the APTS. This data indicates that part of the signal of the incident particle gets lost. This might be the result of traps inside the silicon, excluding the charge from the overall energy deposition, and needs further investigation beyond the scope of this thesis.

5.3.5. Influence of threshold on the cluster size distribution

This section discusses the influence of the threshold set in the data analysis on the cluster size distribution. This parameter is not to be confused with the threshold selected for the data acquisition.



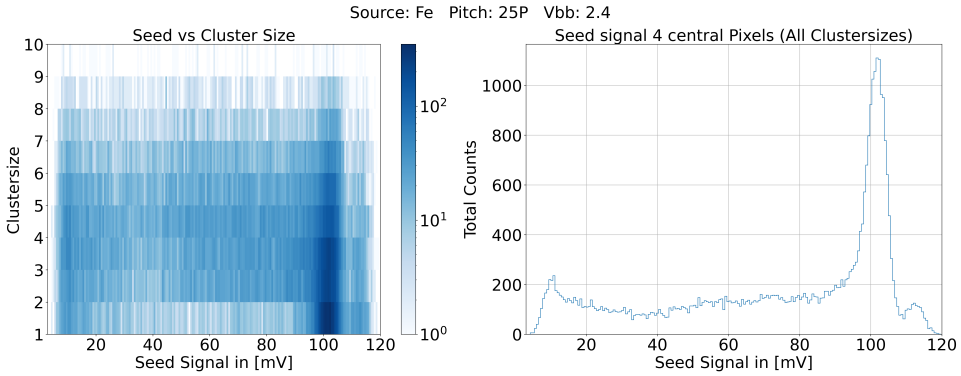
(a) Seed signal vs. cluster size histogram for the calcium measurement with a cut at $1\,\mathrm{mV}$ data applied on the left panel and seed signal spectrum on the right panel



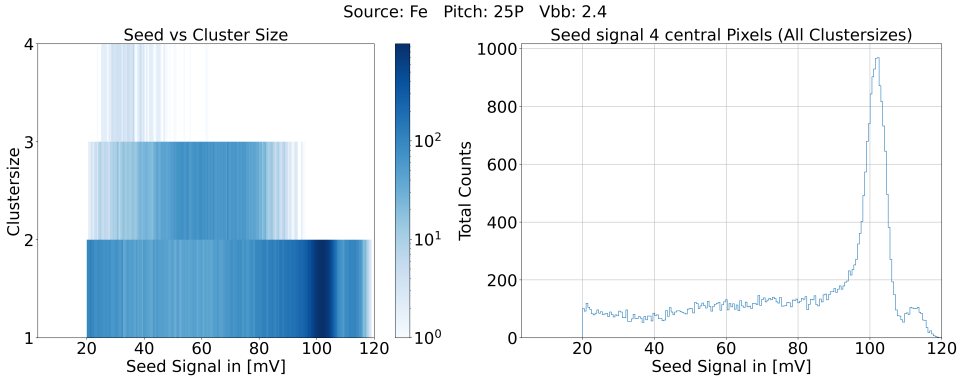
(b) Seed signal vs. cluster size histogram for the calcium measurement with a cut at $20\,\mathrm{mV}$ data applied on the left panel and seed signal spectrum on the right panel

Figure 29 Calcium Spectrum Cluster size vs. Seed signal for the 25 pitch chip: a) Threshold at $1\,\mathrm{mV}$ b) Threshold at $20\,\mathrm{mV}$

Figure 29 & 30 show the cluster size distribution for different seed signals in mV (left panel) as well as the seed signal for the four central pixels with all cluster sizes included (right panel)



(a) Seed signal vs. cluster size histogram for the iron measurement with a cut at $1\,\mathrm{mV}$ data applied on the left panel and seed signal spectrum on the right panel



(b) Seed signal vs. cluster size histogram for the iron measurement with a cut at $20\,\mathrm{mV}$ data applied on the left panel and seed signal spectrum on the right panel

Figure 30 Iron spectra Cluster size vs. Seed signal for the 25 pitch chip: a) Threshold at $1\,\mathrm{mV}$ b) Threshold at $20\,\mathrm{mV}$

for ^{41}Ca and ^{55}Fe, respectively. A cut of $1\,\mathrm{mV}$ was applied to the dataset; see Figures 29a and 30a. This gets compared with the data, in which a threshold of $20\,\mathrm{mV}$ gets applied; 29b and 30b The data acquisition threshold for this measurement was adjusted so that the noise signals occurred at a frequency of about $0.05\,\mathrm{Hz}$. To fine-tune the data acquisition threshold, a measurement has been done without any source. When looking into the data gathered from the ^{41}Ca source, in which the signal-to-noise ratio is high, a clear peak below 10 mV is seen, see Figure 29a, with a cluster size up to 10. Due to the low threshold set, this can be explained by the noise. For the region where the Calcium peak is visible (Mean $56.32 \pm 0.11\,\mathrm{mV}$), the cluster sizes vary from 1 to 8. After applying a cut at $20\,\mathrm{mV}$, the cluster size distribution becomes more sensible. In this case, the Calcium peak has only a cluster size of one event registered. The same is also seen in the peaks for ^{55}Fe. Also, cluster sizes up to 3 can be seen. In this case, all signals of higher multiplicities are below the main X-ray peaks. These events are attributed to charge sharing between pixels. The reason for this change in the distribution of cluster sizes is the algorithm used for clusterization, which is done during analysis. The highest signal is the seed signal. During the same time frame, the next highest signals above the set threshold are searched in the vicinity. If a signal is seen, the cluster size therefore increases. So if the noise is considered for all pixels in the chip, the cluster size distribution can be modified.

6. Summary

The ALICE experiment foresees a major upgrade in the Inner Tracking System (ITS3). The Inner Barrel of the ITS2, consisting of multiple rectangular-shaped staves, will be replaced by 3 layers of silicon chips bent into a cylindrical shape, accounting for the beam pipe geometry. These detectors will be produced with a process called stitching, significantly reducing the material budget by removing the external board (Flexible Printed Circuit), which supplies the voltages/currents and regulates the data outputs. Through this new manufacturing process, wafer-scale silicon chips can be produced. The pixel technology of these silicon detectors is currently under investigation. This work focuses on the Analog Pixel Testing Structure, allowing for waveform studies. Currently, three different implementation layouts (Standard, modified, modified with a gap) and 5 different Pitch sizes ($10\,\mu$m,$15\,\mu$m,$20\,\mu$m,$25\,\mu$m) have been created for the APTS. The principles of operation, as well as the different periphery circuits, have been outlined (Source Follower -SF and Operational Amplifier -OPMAP). The APTS chips studied at TUM are source follower buffer chips equipped with the implantation of the modified process with a gap. Different pixel pitch sizes with varying back bias voltages were compared using an ^{55}Fe source. Charge sharing as well as the effect of different back bias settings, were investigated. Based on the study at TUM, it can be concluded that charge sharing decreases for bigger pixel sizes and bias voltages, and the signals collected from each pixel increase as the back bias voltage increases. The influence of the threshold set for the data analysis and the cluster size distribution has also been studied. A cut-off at $20\,$mV of the seed signal for the calculation of the charge collection efficiency was performed for sensible cluster size distribution. For the comparison of cluster size distributions, a threshold of 300 electrons has been performed separately. Lastly, using a ^{41}Ca radioactive source, a linear energy calibration curve was fitted for the main peaks corresponding to the monoenergetic X-rays from calcium and iron. A clear negative offset from the origin has been observed, which does not vary within the margin of error by applying back bias voltages or changing the pitch size. A possible explanation would be that this is an effect of lost charges due to trapping. A positive offset for the remaining signal, when subtracting the seed signal from the matrix signal, has been observed. This could be the result of the capacitive coupling of the seed pixel with the neighbors. The modified process with a gap provides a substantial reduction of pixel multiplicities for low-energy interactions in the detector at a threshold of 300 electrons. An average pixel multiplicity of 1.2 < m < 1.4 was observed, which indicates a substantial data reduction compared to the ALPIDE chip used in ITS2. In addition, the lower charge sharing guarantees a safety margin for the threshold settings in the detector after substantial radiation damage.

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Appendix

Source	Date of receipt	Initial activity (Bq)	Residual activity (Bq)	Type of source
^{55}Fe	15.03.2011	$1.85 \cdot 10^8$	$9.24 \cdot 10^6$	closed
^{41}Ca	15.10.2019	$2.00 \cdot 10^6$	$2.00 \cdot 10^6$	open

Table 3 Radioactive activity of the sources (Status: 15.11.2022)