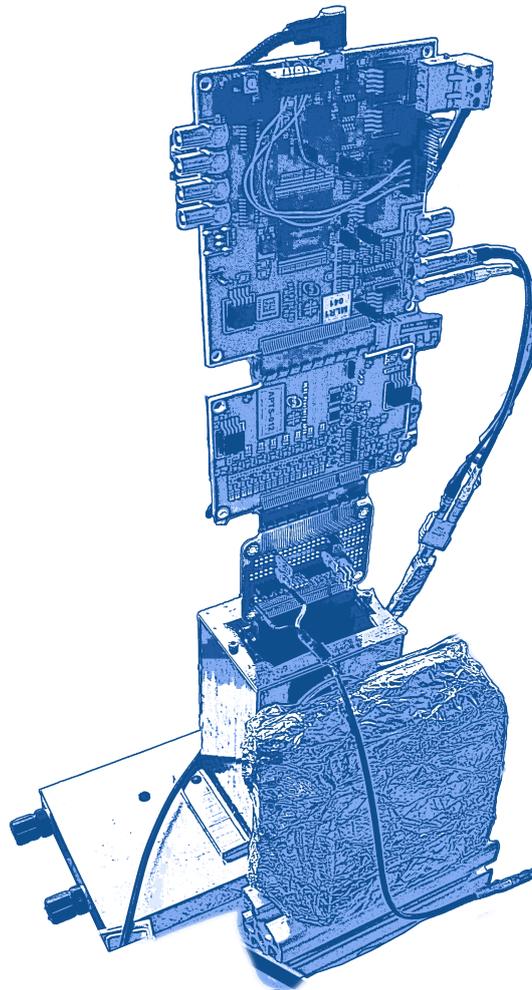


Bachelor's Thesis

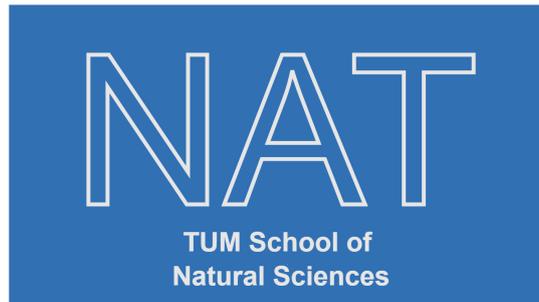
Timing studies for the development of a new silicon detector using CMOS technology at the ALICE experiment

Jan Egger





TECHNISCHE UNIVERSITÄT MÜNCHEN



**Timing studies for the development of a new
silicon detector using CMOS technology at the
ALICE experiment**

**Studie zur Zeitauflösung eines neuen
Siliziumdetektors mit CMOS Technologie für
das ALICE Experiment**

Bachelor's Thesis

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Date: 22.08.2023

I confirm that the results presented in this bachelor's thesis are my own work, and I have documented all sources and materials used.

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Munich, 22.08.2023

Jan Egger

Abstract

The Large Hadron Collider at CERN will undergo major upgrades in the coming years. Improving the existing detectors along its ring and developing new detection technologies is essential to ensure the best possible results can be achieved. One of the key detector technologies considered are CMOS silicon pixel sensors of different doping profiles, different sizes and with different readout systems. A new detection system of this kind is planned for the Inner Tracking System of the ALICE detector. To investigate their properties, a plethora of different test structures have been commissioned. This thesis in particular will focus on the timing resolution capabilities of the modified process with gap variant of the Analog Pixel Test Structure.

The relations between pixel size, bias voltage and their impact on the timing resolution were studied. For all the examined test structures, the observed trends show a better timing resolution for smaller pixel sizes and higher bias voltages. Compared to the timing performance of its predecessor chip ALPIDE, clear improvements of about one order of magnitude can be seen. For all the considered test structures, timing resolution was lower or equal to 1 ns.

Contents

1	Introduction	2
1.1	The Large Hadron Colliders High Luminosity upgrade	2
1.2	The ALICE detector and the High Luminosity upgrade	4
1.3	The Inner Tracking System	5
2	Monolithic Active Pixel Sensors at ALICE	10
2.1	Monolithic Active Pixel Sensors - working principle	10
2.2	The current State at ALICE - the ALPIDE chips	13
2.3	The planned upgrade - the APTS	14
3	Experiment	18
3.1	Timing measurements in general	18
3.2	The Setup	19
3.3	The specifics of the setup	21
3.3.1	The electronics	22
3.3.2	The silicon photomultiplier	23
3.4	Typical measurements and evaluation methods	24
3.5	Time Calibration	25
4	Evaluation of the timing resolution	29
4.1	Trends for different voltages	29
4.2	Trends for different pixel sizes	30
5	Summary and Outlook	31
	List of Figures	32
	List of Tables	34
	Bibliography	35

1 Introduction

In this work we evaluate the timing characteristics of a new pixel detector system for the ALICE experiment at CERN. This chapter serves as an introduction to the specifics of the upgrade of the Large Hadron Collider and the resulting technological upgrades for the ALICE detector system, while shining a light on key challenges and solutions proposed already. Special attention will be paid to the application and key characteristics of the new detector system, in particular its timing resolution capabilities.

1.1 The Large Hadron Colliders High Luminosity upgrade

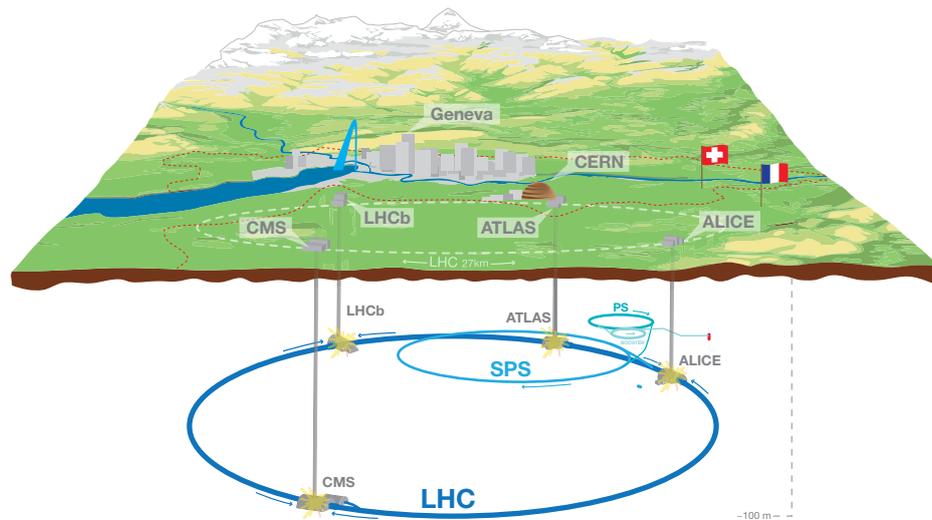
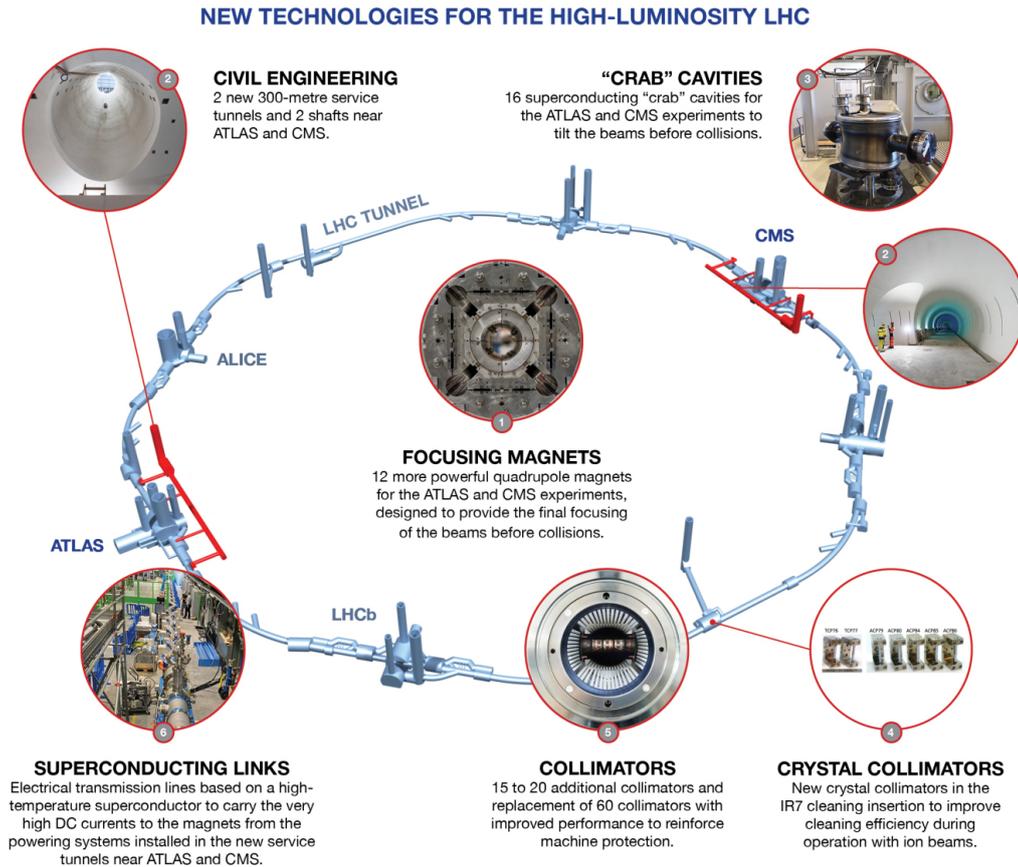


Figure 1.1: Overall view of the LHC, including the ALICE, ATLAS, CMS and LHCb experiments [1]

The **L**arge **H**adron **C**ollider (**LHC**) at lake Geneva, at the CERN, is pushing the boundaries of particle science. As the largest of its kind, it accelerates protons and heavy ions up to 99,9999991% the speed of light or 13 TeV [2] and collides them at one of the four experiments located along its ring 1.1. After its first very successful physics runs in the years 2011 and 2012, which featured the

1 Introduction

breakthrough discovery of the Higgs-boson, long term plans for the LHC were formulated, which were focused on increasing the luminosity. This upgrade, dubbed the **High Luminosity-LHC (HL-LHC)**, aims to provide the scientists at CERN with an increased amount of collisions to study, allowing them to observe low statistics effects to a better precision than until now achievable [3, p. 1]. To achieve this, a wide range of upgrades to existing systems need to be deployed, consisting of, but not limited to, new and improved collimators to focus the beam and high-temperature superconducting links to improve power transport to the accelerator magnets [4]. The main points of the upgrade are shown in figure 1.2.



1.2 The ALICE detector and the High Luminosity upgrade

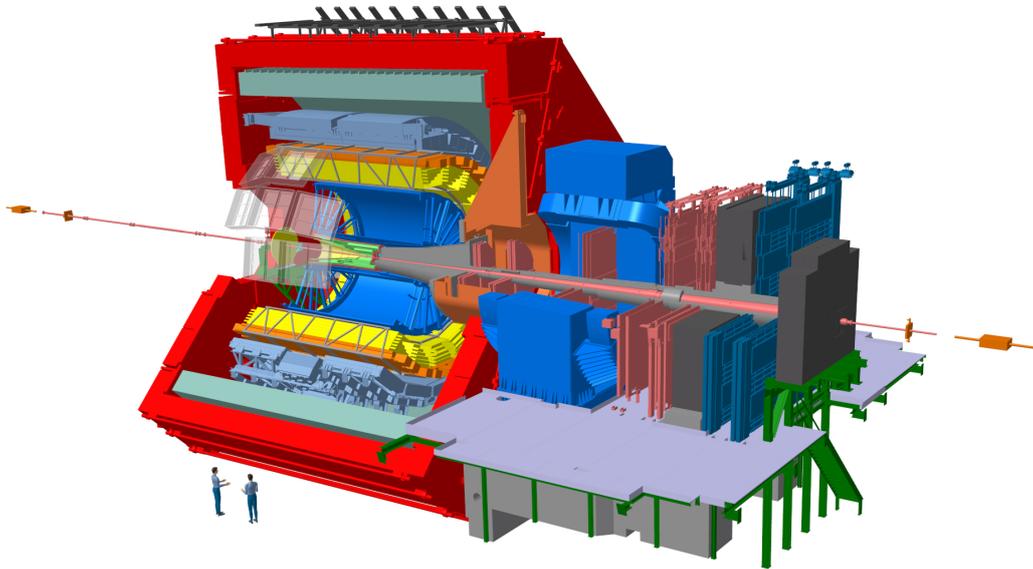


Figure 1.3: Graphic showing the ALICE detector systems, humans for scale [5]

The anticipated increase in luminosity also poses new challenges for the existing detector systems ATLAS, CMS, LHCb and ALICE. Radiation hardness, wear and tear and many other concurring factors make refurbishing or upgrading the existing infrastructure at these experiments necessary. At the ALICE collaboration, for example, preparations for the HL-LHC upgrade are currently ongoing. Besides proofing the detector against the challenges raised by the increased luminosity, the goals of this upgrade include an improved readout rate, pointing resolution, tracking and particle identification for the whole system. To achieve all these goals, a heavy emphasis is put on the development of novel silicon sensors for all parts of the detector. From the large acceptance outer tracker, including the ring imaging Čerenkov detector and time of flight chambers, to the inner tracking system, these silicon chips offer the distinct advantage of high volume production processes, while maintaining the desired performance in regards to tracking, photon detection efficiency, energy and timing resolution. In addition to the hardware upgrades of the detector itself, the injection chain is being closely examined to fully exploit the increased luminosity provided. Lighter ion species than Pb-ions are considered as a replacement, as they would potentially allow for better performance [6, p. 19].

1.3 The Inner Tracking System

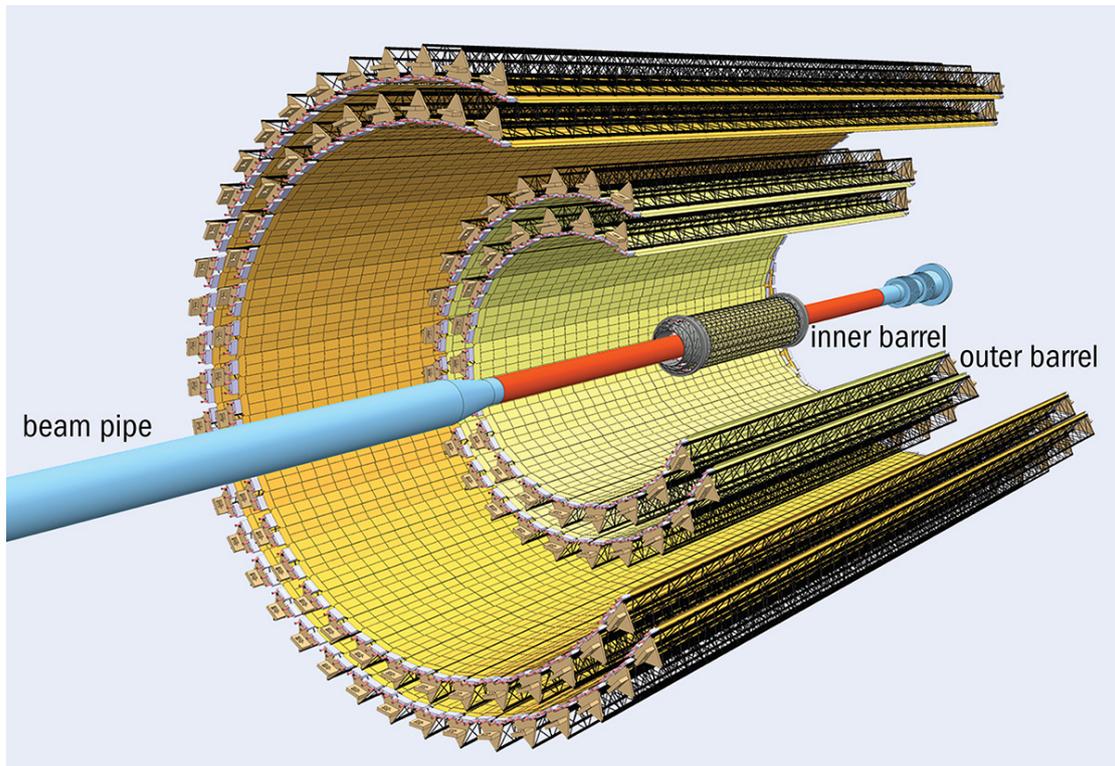


Figure 1.4: Conceptual layout of the previous version of the inner tracking system ITS2 [7]

The first of these upgrades to be implemented is the upgrade of the **Inner Tracking System (ITS)**. The currently deployed, second version, called ITS2, is the result of 8 years of research and development of the ALICE collaboration and allows for nearly 4π tracking capabilities. Conceptually it consists of an outer and an inner tracking system, called **Outer** and **Inner Barrel (OB/IB)**, as can be seen in figure 1.4. Each of those barrels is then separately made up of smaller tracking layers of **Monolithic Active Pixel Sensors (MAPS)**, four for the OB and three for the IB. These layers are each then mounted on staves, which consist of 3 main parts providing different kinds of support [8, p. 4]:

1. **Space Frame:** a carbon fibre support structure providing the mechanical support and the necessary stiffness
2. **Cold Plate:** a sheet of high thermal-conductivity carbon fibre with embedded polyimide water-cooling pipes, it is in thermal contact with the Pixel Chips
3. **Hybrid Integrated Circuit:** an assembly consisting of a polyimide flexible printed circuit onto which the Pixel Chips and some passive components are bonded.

1 Introduction

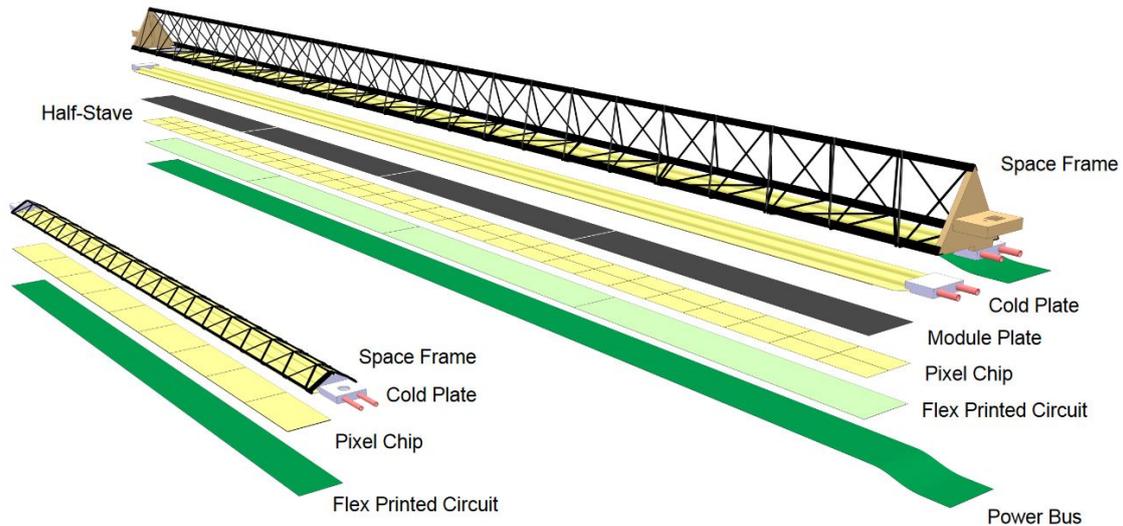


Figure 1.5: Schematics of IB (left) and OB (right) staves. Even though IB and OB staves have different geometries, both have the same core features [9, p. 13].

These supporting staves come at a high cost for the material budget, increasing its mean radiation length to 0.35% of the mean radiation length X_0 . Thereby the amount of multiple scattering, which negatively impacts measurement precision, is increased. Consequently, a reduction in the material budget is one of the main challenges for any new detector systems. In the ITS2, the main contribution to the material budget stems from the electric circuitry and its connections to the Pixel chips. Kapton, used for electrical insulation, and the glue used for mechanical support of the bonding, together with the other components of the wiring, account for nearly half of the material used. Another 35% of the material is allotted to cooling and mechanical support components, mainly cooling-water, aluminium and carbon support structures [8, p. 5]. A detailed distribution of the material along the azimuthal angle, with respect to the individual contributors can be seen in figure 1.6. In this graphic another problem of the stave as a mean of construction is clearly shown. As the staves are rectangular shaped they need to be layered to cover a full azimuthal angle of 4π . This is visible for example in the sharp peak at 0° in the material distribution 1.6. Interestingly the only active physics component, the silicon detector chips, account for just about 15% percent of the total material used. Therefore significant reductions can only be achieved by reducing the amount of external circuitry and cooling needed to sustain operations [8, p. 5].

During the test phases of the ITS2 it was already shown that significant reduction of cooling material could be realised utilising only constant airflow instead of water, if the power consumption of the total setup would not cross a threshold of $20 \frac{mW}{cm^2}$. This operative iteration of the ITS2 has a power consumption of around $40 \frac{mW}{cm^2}$ which in addition is not split evenly across all different parts. While the silicon detectors internal power consumption can be fixed at around $7 \frac{mW}{cm^2}$, the digital interface circuitry and the high-speed output data links located at the border of the active elements account for the bigger part of the heat output of the system [6, p. 6].

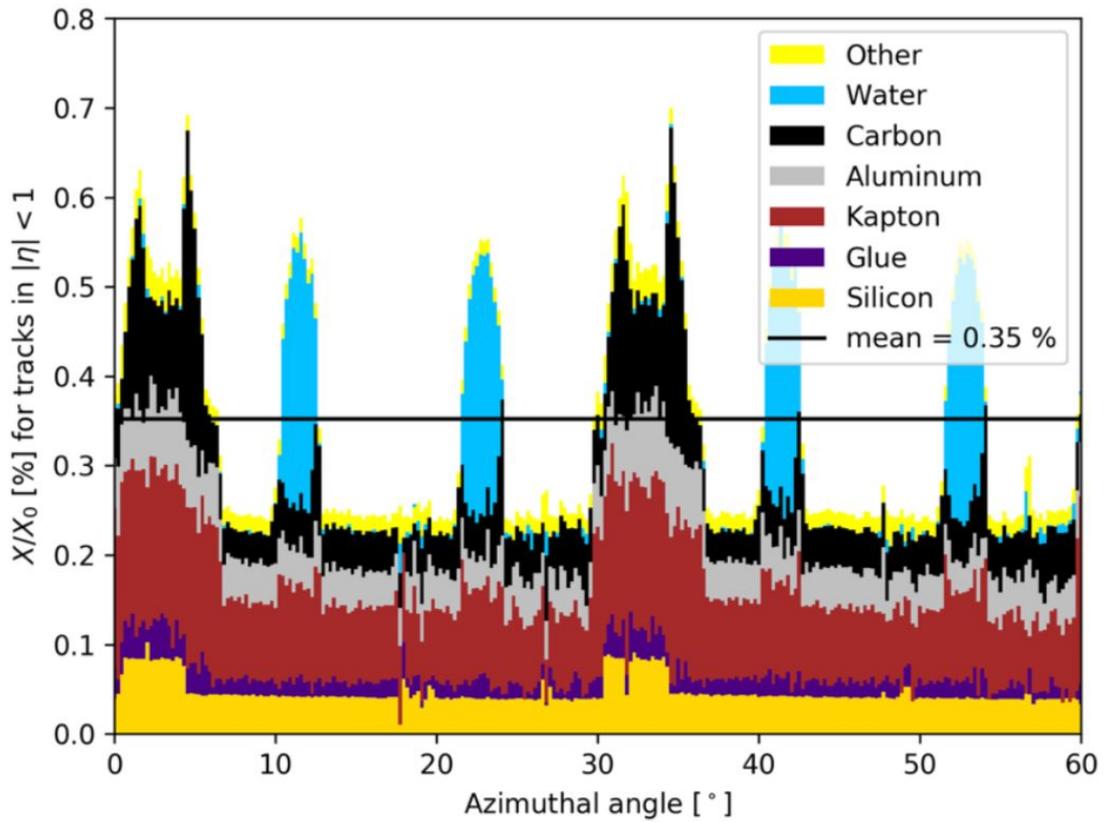


Figure 1.6: Azimuthal distribution of the material of layer 0 in terms of radiation length [8, p. 7]

The planned upgrade, ITS3, is designed to match the new requirements in material budget and data acquisition by employing two new key technologies. Complementary Metal-Oxide-Semiconductors (CMOS) in combination with stitching would allow to construct bent sensors with internal power and data distribution of which two would cover the area currently covered by a ITS2 inner barrel. These bent sensors would only be installed in the IB of the current ITS system while the OB from the ITS2 would remain in use. For this, a new barrel layout was proposed, which can be seen in figure 1.7. It consists of 2 half barrels supported by a cylindrical structural shell. Each of those half barrels is individually made up of three layers of new stitched detector chips, with true cylindrical geometry to allow for 4π coverage.

1 Introduction

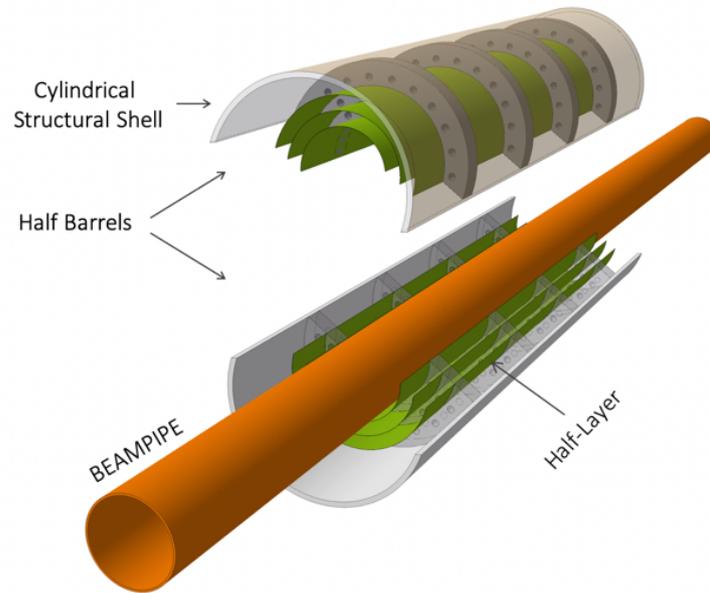


Figure 1.7: The proposed layout of the IB of the new ITS3 utilising bent silicon chips and carbon foam for support [8, p. 10]

The proposed electronic readout and the power supply, the main heat generator of the previous ITS iteration, will take place far away from the active material of the sensor, thus greatly decreasing the power consumption and heat generation inside the tracking system. All these measures together will allow to reduce the material budget of the new ITS to $0.2\text{--}0.4\% X_0$ [6, p. 9], approximately a tenth of the material currently used for the ITS2 [8, p. 9].

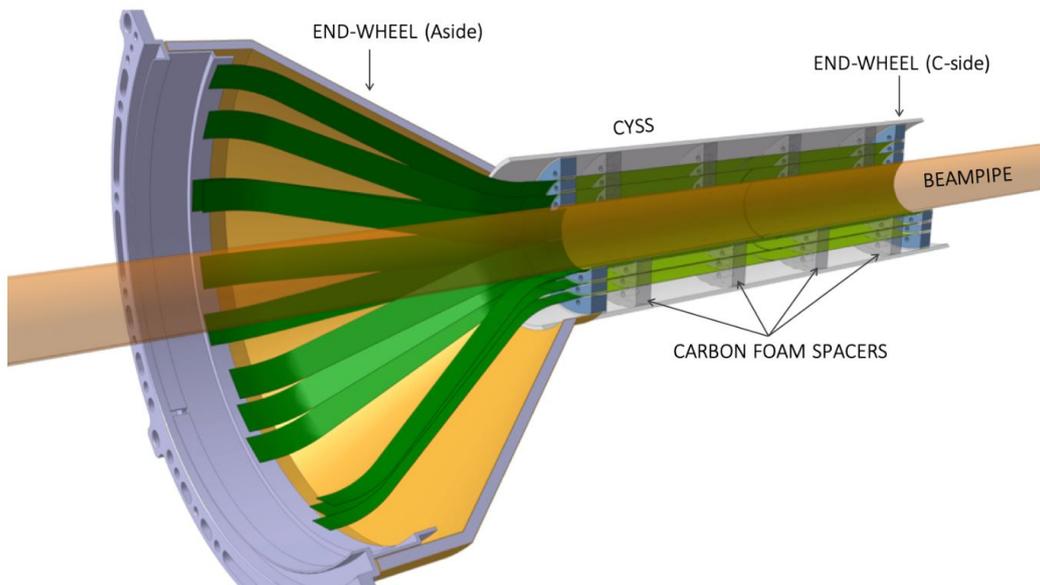


Figure 1.8: The proposed electronic readout and power supply endcap for the ITS3 [8, p. 11]

1 *Introduction*

While the reduced heat generation and the resulting possibilities to reduce the material budget are a big improvement in the proposed version of the ITS3, the sensors together with their readout electronics will also undergo significant changes. A key feature of those upgraded pixel sensors will be a reduced pixel size, also called pitch, by a factor larger than two. This will improve the pointing resolution and the charge collection time, which in turn, benefits the readout rate capabilities, radiation hardness and potential timing resolution of the system [8, p. 9].

Whereas radiation hardness and timing resolution are not the main objectives of the new detector systems at ALICE, new technological advancements in manufacturing silicon pixel detectors, will nevertheless impact a broad range of experiments. To explore these experimental technological applications, the experimental physics department at CERN, more specifically the research and development on experimental technologies department, accepted contributions regarding the testing of timing resolutions for one type of pixel detector, the **Digital Pixel Test Structure (DPTS)**, considered for the ALICE upgrade [10, p. 22]. The goal of this work is to characterise another version of a pixel detector considered for the ALICE upgrade, the so called **Analogue Pixel Test Structure (APTS)**, with regards to its timing capabilities.

2 Monolithic Active Pixel Sensors at ALICE

The goal of this chapter is to give a basic understanding of **Monolithic Active Pixel Sensors (MAPS)** and introduce key aspects of old and new versions of MAPS present and planned for the ALICE experiment.

2.1 Monolithic Active Pixel Sensors - working principle

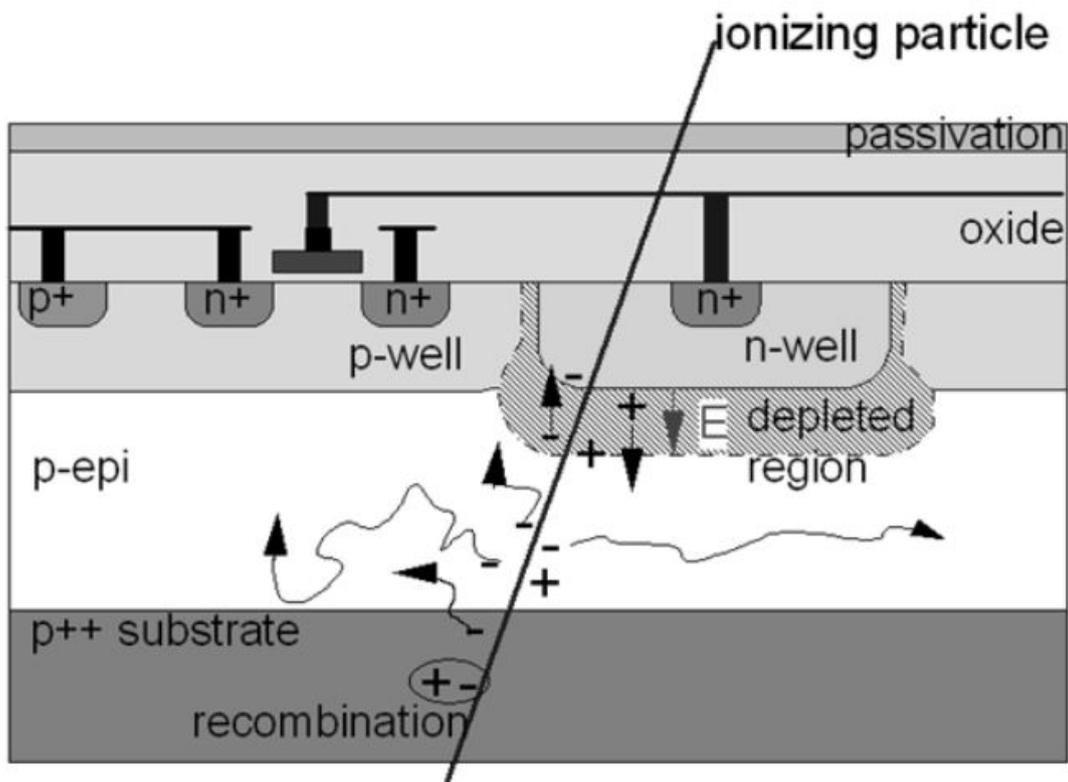


Figure 2.1: Schematic working principle of a MAPS-epi sensor [11, p. 10]

Monolithic Active Pixel Sensors (MAPS) combine readout circuitry and active Si diodes and allow for fabrication in some standard **Complementary Metal-Oxide-Semiconductor (CMOS)** processes. This allows for crucial advantages over comparable hybrid sensors as they are a) cheap to build, even in large array sizes, b) can be thinned down, in case of the ITS3, to allow for bending, c) still allow individual pixel readout and d) have the needed radiation hardness and low-mass. Furthermore, they can be operated at high speeds with low power consumption, from a

single and low voltage supply [12, p. 2]. These key features make the MAPS an attractive choice for the ITS3 upgrade and high-energy physics in general [11, p. 11].

There are many different kinds of MAPS, based on different kinds of approaches and degrees of unification of the readout circuitry and the detection layers. These techniques include, for example, the **Silicon on Insulator (SoI)** technique. Here the conductive layers from the transistor are insulated utilising a thin layer of SiO_2 . Another technique, the **MAPS-epitaxial**, exploits the common occurrence of a thick epitaxial layer in between the silicon substrate layer and the CMOS electronics layer, to isolate the electronics from the active material. As the pixel detectors used in ALICE are MAPS-epi we will focus exclusively on those.

The working principle of a classical MAPS-epi device, as is planned for the ITS3 and currently deployed in ITS2, is visualised in figure 2.1. Ionising radiation generates a charge in the active regions of the pixel, in this case the p-epitaxial layer [11, p. 11]. In order to shield the readout electronics from these electric charges, there is a deep n- or p-well (as is the case for the ITS3) protecting the transistors used for further signal processing from these influences [11, p. 10]. A scheme of this, similar to the one to be used in ITS3 can be seen in 2.2.

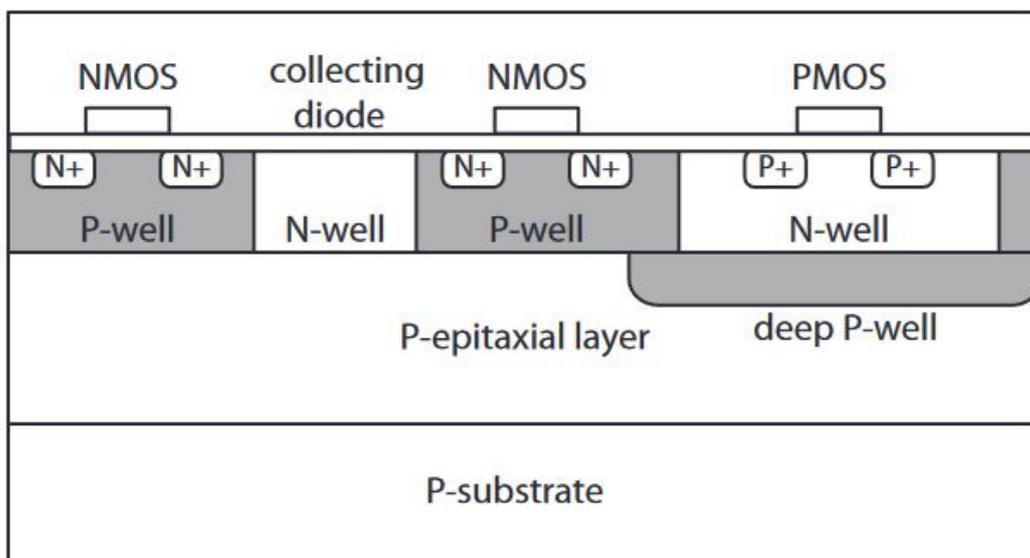


Figure 2.2: Scheme of a deep p-well shielding. The n-well contains the signal processing units [11, p. 10]

The next step, collection of the generated charge, can be described by two main mechanisms, thermal diffusion of generated charges and drift in an electric field, called depletion zone. This is generated by a collection diode, the n-well in figure 2.1. Thermal diffusion inside the silicon lattice is a random process not controlled by a strong force and prone to trapping of the charges

in defects, increasing the readout time up to several 100 ns. As the number of defects increases with irradiation level, radiation tolerance further decreases making this way of collection sub optimal. To counter this problem, the development of newer sensors is focused on utilising drift in a depletion zone, as space-filling as possible. The desired result is a faster, more efficient charge collection, which coincides with a lower charge sharing in between adjacent pixels [13, p. 2]. The main metric to classify the different kinds of MAPS is the Signal-to-Noise ratio ($\frac{S}{N}$). This ratio provides information about the mean signal amplitude in comparison to the mean noise amplitude. As such a $\frac{S}{N}$ ratio of one indicates that signal and noise have the same amplitude. For detector applications a $\frac{S}{N}$ ratio as high as possible is desired to pick up as small signals as possible. A key factor in calculating the $\frac{S}{N}$ ratio, is the proportion of signal charge Q to pixel sensors capacitance C . The power consumption P is related to $\frac{Q}{C}$ by the following equation[13, p. 4]:

$$P \propto \left\{ \frac{Q}{C} \right\}^{-m} \quad \text{with} \quad 2 \leq m \leq 4$$

According to this relation, optimisation of the $\frac{Q}{C}$ parameter allows to reduce the supplied power, while keeping the analogue performance the same [13, p. 4]. This can be achieved in two different ways, by either increasing the charge deposited or by decreasing the capacitance of the detector. As charge deposition is highly dependent on the kind of ionising radiation used and thus not a useful parameter, the pixels capacitance is the better choice for optimisation. To first order, the capacitance of the pixels can be approximated using the well known formula for spherical capacitors, by assuming the N-well as the inner sphere with radius R and distance of the outer boundary of the space charge region, or depletion area as r :

$$C = 4\pi \cdot \epsilon \cdot \epsilon_0 \cdot \frac{R \cdot (R + r)}{r} \approx 4\pi \cdot \epsilon \cdot \epsilon_0 \cdot \frac{R^2}{r} \quad \text{for small } r$$

Increasing the distance r between the N-well and the outer border of the space charge region, allows for an immediate reduction in capacitance and therefore power consumption. But this is not the only advantage of a larger space charge region. A larger electric field region directly corresponds to a larger drift region inside the pixel, improving charge collection time, efficiency and reducing undesired effects such as charge sharing [14, p. 2]. This is of utmost importance to the final timing resolution of the pixel detector. Therefore present and future MAPS for high-energy physics try to maximise this depletion area with different approaches.

2.2 The current State at ALICE - the ALPIDE chips

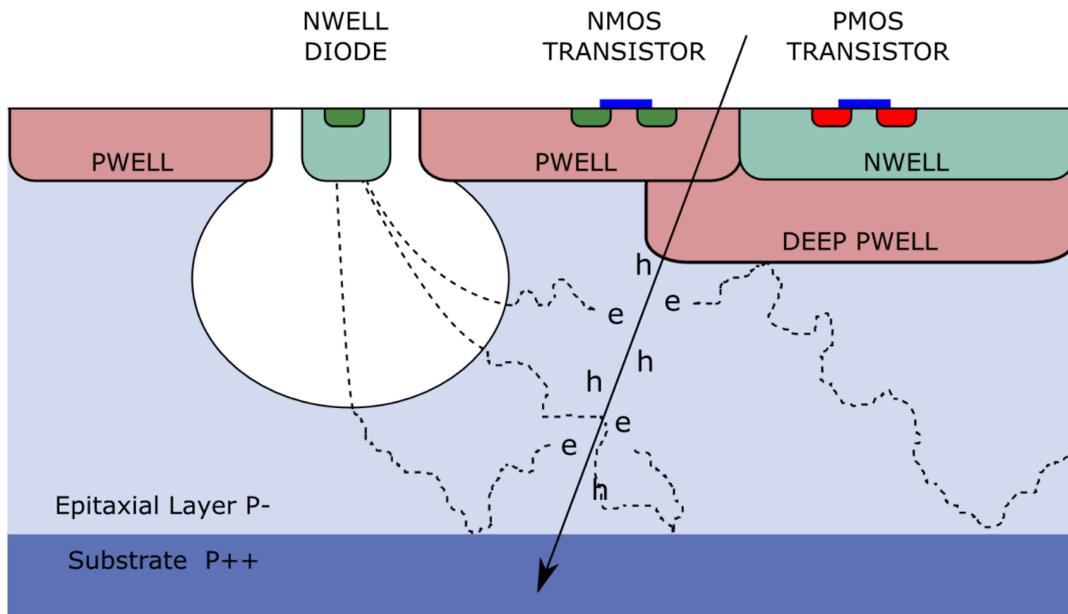


Figure 2.3: Scheme of ALPIDE sensor doping profile, with deep P-well to shield the signal processing electronics [15, p. 2]

The first iteration of pixel detectors in use at ALICE are the so called **ALICE Pixel Detector (ALPIDE)** chips. Produced in the TowerJazz 180nm CMOS imaging process, they are an MAPS-epi with a transistor feature size of 180nm. They utilise the full range of technologies discussed in section 2.1, including a deep p-well shielding the readout and processing circuitry, allowing for extended circuitry on the surface of the detector. This readout circuitry consists of a continuously active discriminating amplifier and a multiple-event memory into which data can be saved and later read out [15, p. 2]. The former, is the main contributor to the timing resolution and increases it to $2\text{-}4\mu\text{s}$ [16, p. 1].

Figure 2.3 shows the so called "standard process" production-variant of the ALPIDE sensor. This standard process features only a single n-well diode and a high resistivity epitaxial layer, allowing for application of small reverse bias voltage, the so called backbias voltage (V_{bb}), in the range of 0V to 5V in between the substrate layer and n-well diode. Applying this V_{bb} increases the size of the depletion region [17, p. 2], indicated by the white blob in figure 2.3. As can be seen, it does not cover the whole epitaxial layer.

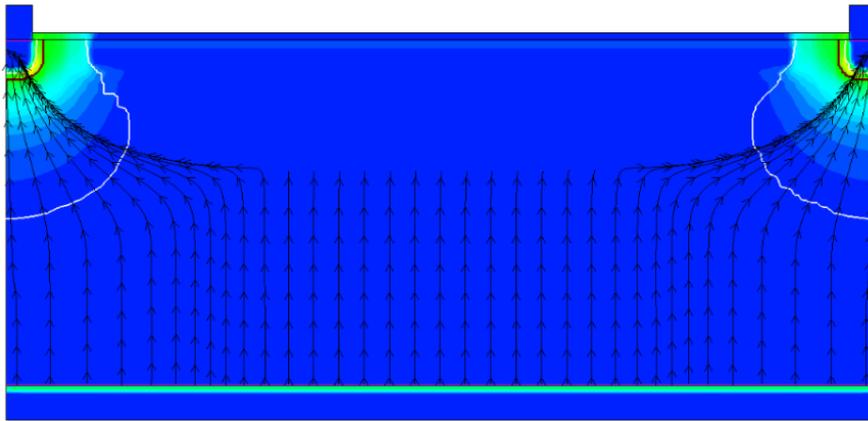


Figure 2.4: TCAD Simulation: electric field for the standard process, applied V_{bb} of 4.8 V [18, p. 4]

Taking a closer look at the electric field generated by this process, visible in figure 2.4 for a V_{bb} of 4.8V, nearly the maximum possible voltage, shows a clear area of possible improvement. The charges generated in the region in between the two pixels, which are located in the upper right and upper left had corner, are not guided into one of the 2 adjacent collection diodes by the electric field. This results in unwanted charge sharing in between adjacent pixels and consequently, negatively impacting the charge collection time and therefore the timing resolution.

2.3 The planned upgrade - the APTS

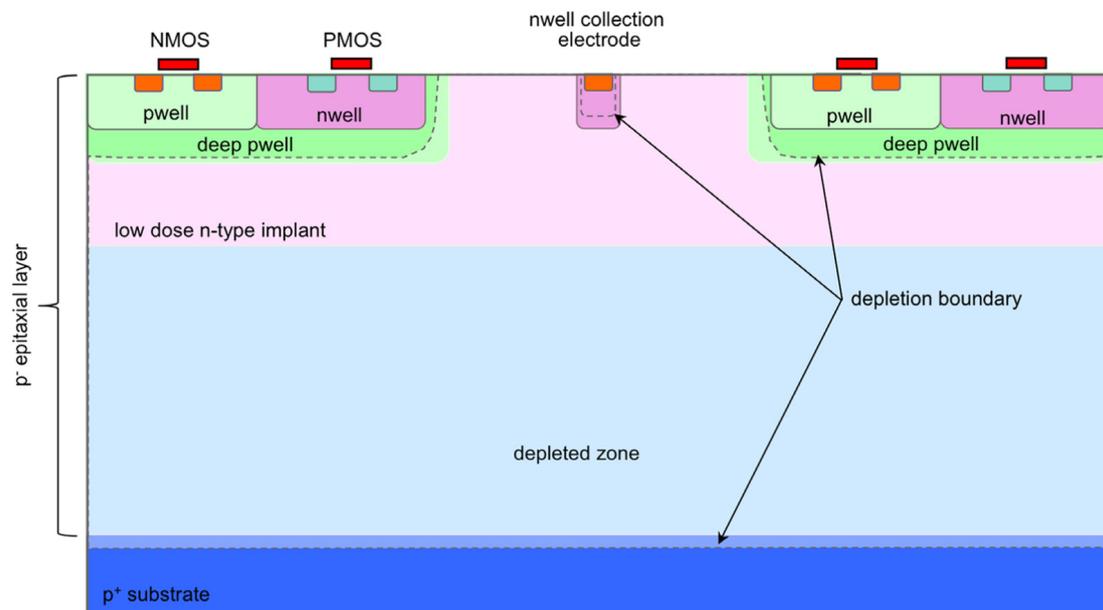


Figure 2.5: A low dose n-type blanket is introduced to improve performance [14, p. 4]

To counter the problems mentioned in section 2.2 in the ITS3, the first step was the modification of the existing doping profiles to increase the depletion zone with the goal of covering the full epitaxial layer. The first attempt, the so called modified process, is shown in figure 2.5. A low dose n-type implant separate from the collection diode was implemented across the whole epitaxial layer, allowing for a small collection electrode to decrease capacitance, while simultaneously featuring nearly complete depletion of the epitaxial layer even at 0V V_{bb} [14, p. 3]. Fully Depleting the n-type blanket layer charges then only requires a low V_{bb} to achieve, indicated by the captions in figure 2.5.

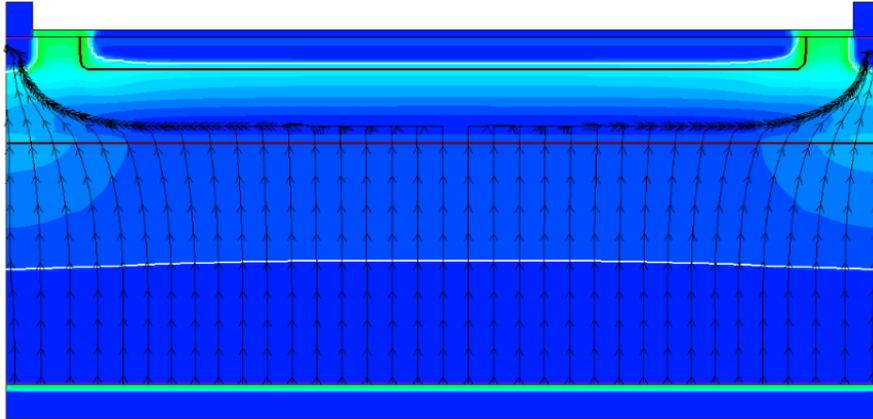


Figure 2.6: TCAD Simulation: electric field for the modified process, applied V_{bb} of 4.8 V [18, p. 4]

Comparing the electric field now created by the modified process in figure 2.6 to the electric field of the standard process 2.4, clear improvements can be seen, but one crucial problem persists. In the middle in between the n-well diodes a small gap, in which the field is still zero can be seen. In this area charge depletion is again governed by diffusion, resulting again in a slower charge collection, increasing the chances of trapping and decreasing charge collection efficiency. Furthermore this effect decreases the detection efficiencies at higher irradiation levels [19, p. 4].

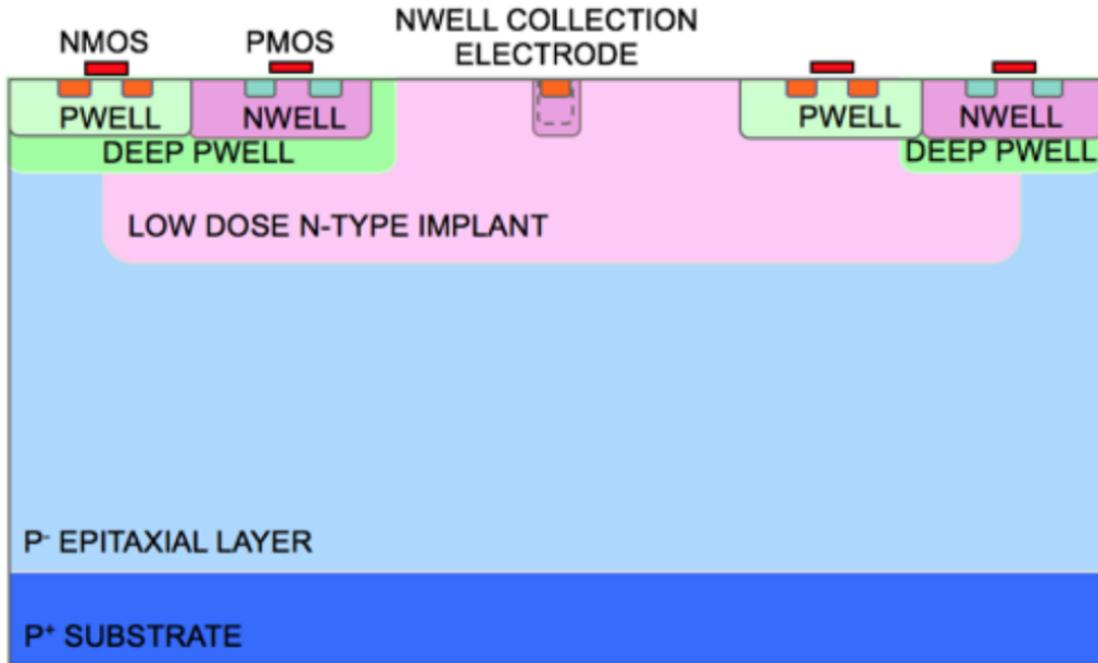


Figure 2.7: A gap in the low dose n-type blanket is introduced, creating a lateral field [20, p. 7]

Reduction of the size of the zero field region was the goal of the next variant called the modified process with gap, visible in figure 2.7. This version features a little gap in between the low dose n-type blankets to create a small lateral electric field. This electric field, as can be seen in figure 2.8, further decreases the size of the zero field region [19, p. 5].

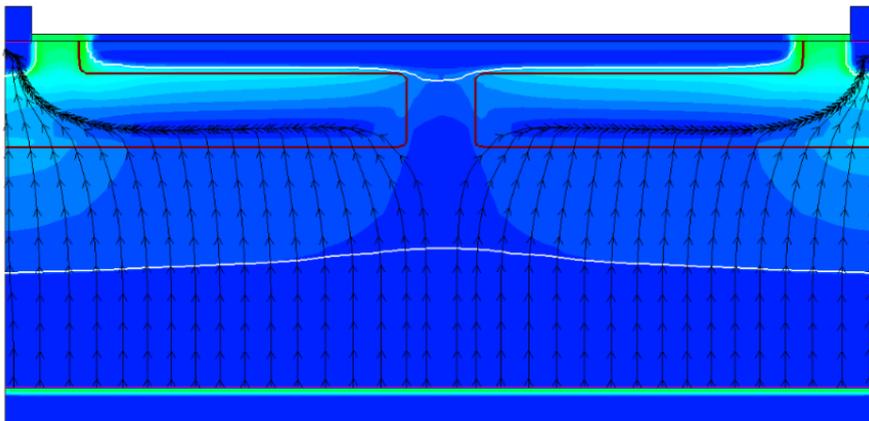


Figure 2.8: TCAD Simulation: electric field for the modified process with gap, applied V_{bb} of 4.8 V [18, p. 4]

To experimentally verify the results obtained through simulations and potentially observe unforeseen effects with the new doping profiles, a wide range of test structures with different pixel sizes and oping profiles was commissioned. In contrast to the preexisting ALPIDE sensor, utilising a 180nm process, the new and improved pixel detector test systems were manufactured on a 65nm process CMOS imaging process. This increases the pixel logic densities possible and

further reduction in material thickness [14, p.1]. The different types of test structure can be seen in figure 2.9.

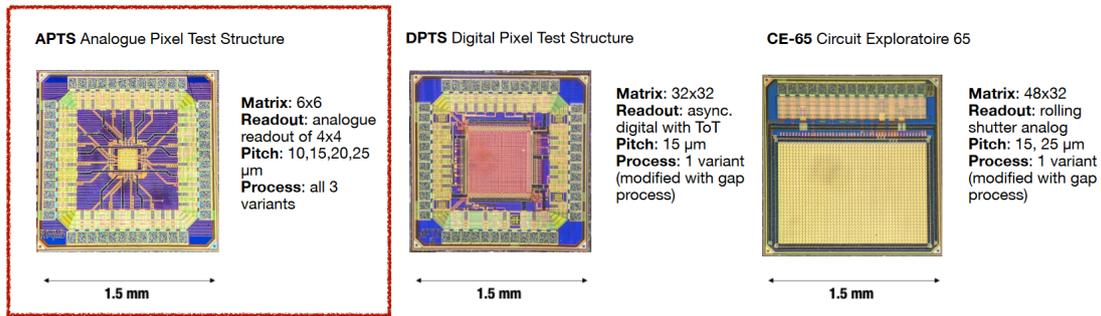


Figure 2.9: All available test structures, the APTS is marked in red[21, p. 5]

Besides the APTS and DPTS, the third test structure implemented was the so called **Circuit Exploratoire 65nm (CE65)**. In the framework of this thesis, experiments were only conducted using the APTS. While all three different kinds of doping structures were available for this chip, only the modified with gap version was used in this work, as this promised the best possible performance. It features a 1.5 by 1.5 mm square shape with a 6 by 6 pixel matrix in its centre. Of this only the inner 4 by 4 matrix was active, the outer ring only existing to eliminate possible border effects. The different pixels inside this matrix are numerated in accordance to figure 2.10.

0	12	15	3
4	9	10	6
13	14	10	15
11	7	6	3

Figure 2.10: Pixel numeration of the APTS inner 4 by 4 matrix, used pixels in green

Its timing resolution was analysed for the pixel sizes 10 μm , 15 μm , 20 μm and 25 μm , also referenced as pitch sizes. For each of these pitch sizes, only the pixel 9 and 10 were used to measure the timing resolution, as these lie in the centre of the 4 by 4 matrix reducing possible effects resulting from inactive pixels. Furthermore the choice was made to investigate two pixels per pitch size to eliminate effects occurring only on a single pixel and thereby improve the accuracy of the timing resolution measurements.

3 Experiment

In this chapter we explain the experimental procedure used and statistical uncertainties and errors arising from the setup. Furthermore we detail the means of obtaining and analysing the data to gain an understanding of the resulting timing resolutions.

3.1 Timing measurements in general

For this experiment a tried and true approach for timing resolution measurements, analogue to [22], was chosen. The detector to be surveyed is placed as close as possible in front of a second control detector. If this construction is aligned with a source of fast particles, most commonly either from a particle beam or a radioactive source, depending on availability, the time delay between the control detector and the test detector allows for a calculation of the timing resolution. An important parameter to control is the energy deposited in the detector systems, as this impacts the signal height and thus the rise time of the detectors. Whereas using a beam the energy deposition of the fast moving particles can very accurately be tuned by changing the beam parameters, radioactive sources do not offer this advantage and thus have to be carefully chosen to mimic the circumstances during the intended use of the detector. In the next step, the signals from both of the detectors are processed further. At first they are amplified and then separately fed into a **Constant Fraction Discriminator (CFD)**, which inverts, attenuates, delays and finally adds each incoming signal waveform. The superposition of the inverted and the original waveform creates a zero crossing, independently of the amplitude of the incoming signal. The zero crossing defines the time of arrival [23]. The two outgoing timing signals, one from the test and one from the control detector, are then used as start and stop signal respectively, of a **Time to Amplitude Converter (TAC)**. This device transforms the delay in between a start and a stop signal into an outgoing signal amplitude proportional to the time delay [24]. The TAC signal is read out and converted into a spectrum by a **Multi Channel Analyzer (MCA)**. In the MCA the signals are sorted into bins according to their pulse height, thus creating a time spectrum from which the time resolution can be computed [25].

3.2 The Setup

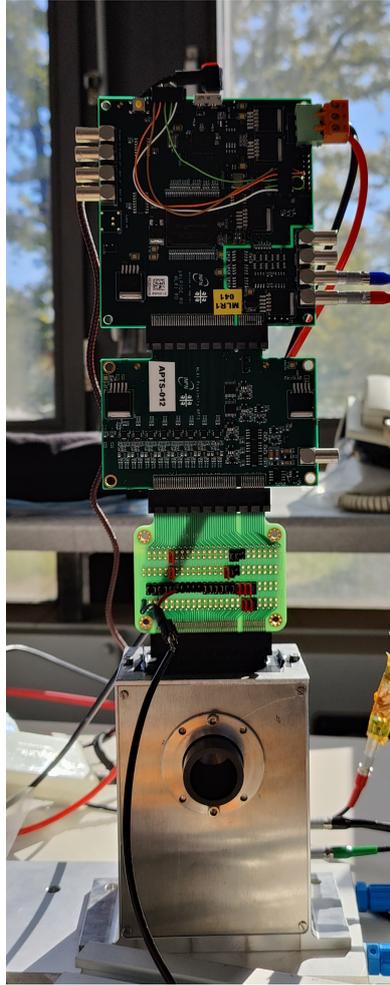


Figure 3.1: Picture of the housing of the setup together with the readout electronics. From top to bottom: DAQ board, proximity card and breakout board, green cable for SiPM signal, frontal cable out of breakout board for APTS signal

The setup used for this experiment strictly follows the description given in section 3.1. As our test detectors, the APTS chips, are very fragile and sensitive to photons, an enclosed housing for the detectors was constructed. The readout and control electronics were situated right above the housing box as can be seen in figure 3.1. Special attention should be paid to the breakout board, built for this kind of measurements. Situated right above the box and before the proximity board and FPGA controls in the **Data AcQuisition (DAQ)** board, it allows to extract the single pixel signal of pixel 9 and 10, their position can be seen in 2.10. Choosing these two different pixels per test detector has two distinct advantages. First, anomalies occurring only on a single pixel can be excluded and second, their placement within the test structure allows to neglect eventual border effects with the **Printed Circuit Board (PCB)**. The control detector in our case consists of a plastic scintillator and a **Silicon Photo Multiplier (SiPM)**, which provides an excellent time resolution for all used ionizing particles. Due to a lack of available particle beams, a radioactive

3 Experiment

β -source, namely $^{90}_{38}\text{Sr}$ was chosen. With a β end point energy of about half a MeV [26], its energy deposition in silicon can be computed using the Bethe-Bloch-Formula [27] resulting in an approximate energy deposition of 5 keV in the detector. This is very similar to protons at 2-3 GeV, which would deposit similar amounts of energy [27] and mimics its intended use case. The dimensions of the housing and especially the distances in between the detectors inside and the source, can be seen in figure 3.2. As the particles emitted by the $^{90}_{38}\text{Sr}$ sources have velocities close to the speed of light, and the distance is in the order of mm, the delay resulting from the geometrical distance is negligible for the total timing resolution of the system.

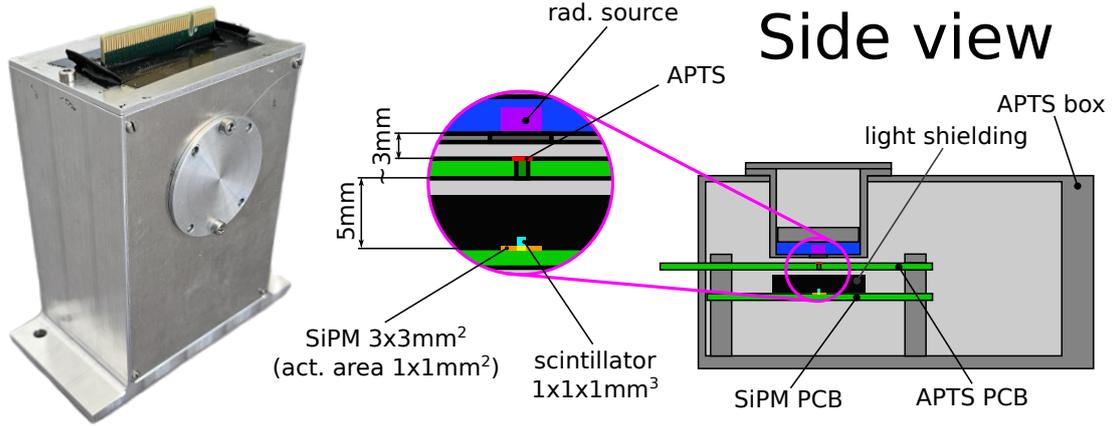


Figure 3.2: Scheme of the inside of the housing with distances in mm

The signal of the SiPM is extracted from the side port of the housing and the APTS signal from the breakout board. Both signals are subsequently amplified using an AvanteK GPD-401 amplifier. This amplifier has a stable gain of about 15 dB across its whole spectrum from 5 Mhz up to 600 Mhz [28, p. 7]. This large range of operations allows the amplifier to increase the signal while still keeping its intrinsic properties.

As described in section 3.1, the signals are fed to a Ortec QuadCFD CF4000, with a pulse pair resolution of 15 to 20 ns [29, p. 18], largely sufficient for the expected pulse pair distance of a single detector in the order of tens ms. As the delay in between the two signals from the detectors directly corresponds to the fraction, that is calculated as the zero crossing, identical length delay cables were chosen for both of the signals. To sort out unwanted background signals the noise threshold level was set individually for both detectors [29, p. 2]. It was tuned to 150 mV for the APTS and 70 mV for the SiPM, as both feature different levels of noise.

The CFD signals were send as start and stop input into a Ortec 467 TPHC/SCA. To optimise the time-range of the TAC used and achieve optimal precision, the stop signal from the SiPM was delayed by about 20 ns using a cable and the TAC set to a range of $0.2 \mu\text{s}$ as a time-range of possible delays. This results in a resolution of $<0.01\%$ of FWHM for the outgoing signal [30, p. 9]. Looking at the outgoing signal, it ranges from 0V to 10V depending on the ratio of the delay in between the start and stop signal in regards to the time range of the TAC, which in our case would be about 10%, so around 1V.

The MCA used to turn the TAC signal into a time spectrum is a MCA4 by FastComTec. It is used in the **Pulse Height Analysis (PHA)** mode, which sorts the signal in one of the 16k bins

3 Experiment

according to their pulse height. This can happen with a frequency higher than 1M events per second, which far outperforms our rate of events [31, p. 2]. The output spectrum was then saved for further analysis using the proprietary MPANT software[31, p. 3].

The full resulting scheme of the circuit with all its components can be seen in figure 3.3

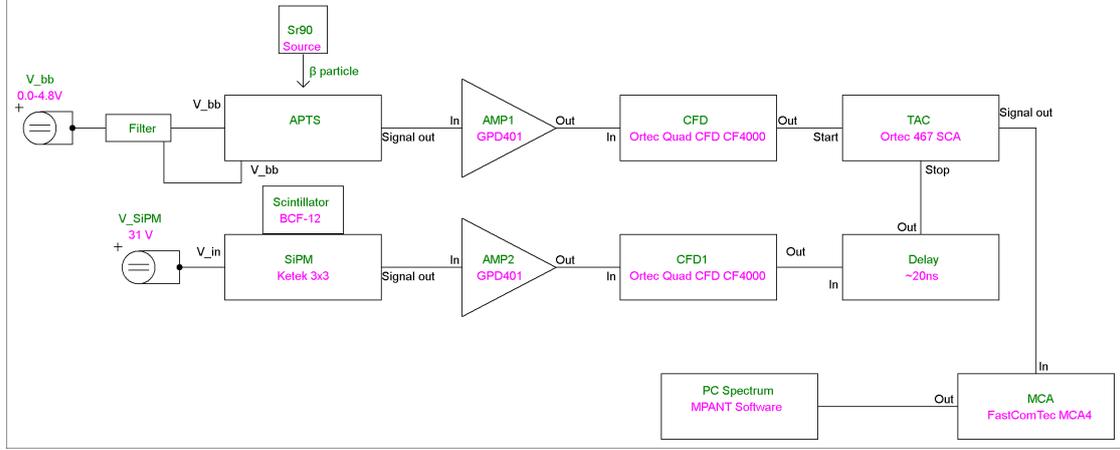


Figure 3.3: Circuitry used to measure the timing resolution

3.3 The specifics of the setup

$$\sigma_{measured} = \sqrt{\sigma_{APTS}^2 + \sigma_{SiPM}^2 + \sigma_{Electronics}^2} \quad (3.1)$$

As every part of the setup described in section 3.2, has its own internal time resolutions contributing to the total resolution described in equation 3.1[23, p. 6]. In this equation:

1. σ_{APTS} : is the contribution of the APTS chip tested, the final quantity to be calculated
2. σ_{SiPM} : is the contribution of the SiPM control detector, which has to independently measured, see section 3.3.2 for details
3. $\sigma_{Electronics}$: is the contribution of the electronics resulting from unknown capacitances and intrinsic resolutions of the devices used, which has to independently measured, see section 3.3.1 for details

As these unknown factor can pose significant contributions to the timing resolution, it is important to measure this information to finally compute the timing resolution of the APTS chips.

3.3.1 The electronics

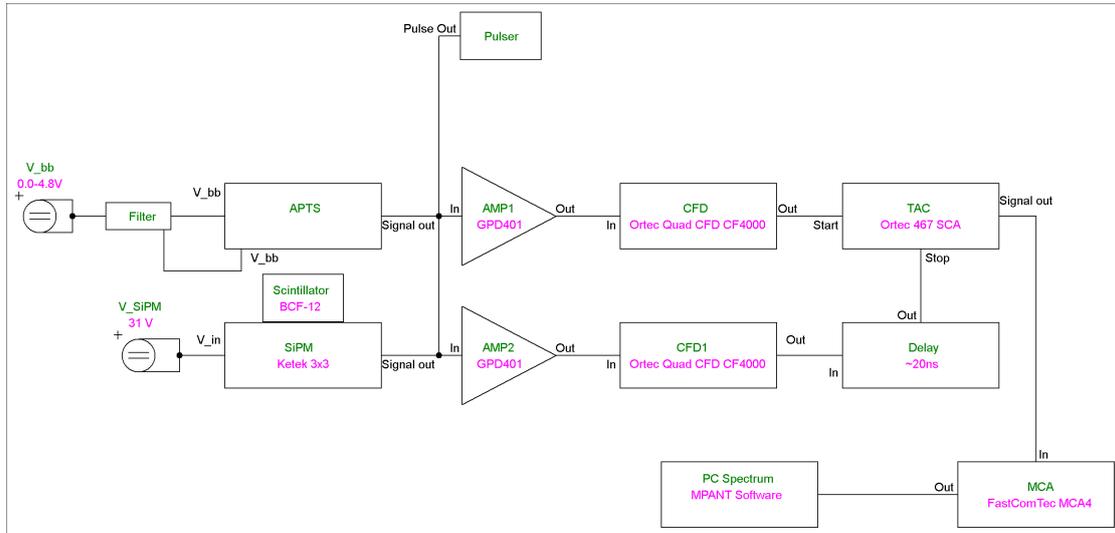


Figure 3.4: Circuit scheme of the configuration used to measure the internal timing resolution

To measure the timing resolution of the electronics a pulser was introduced between the amplifiers and the detectors, as can be seen in figure 3.4. The goal was to simulate a detector signal in the rest of the electronics and thereby allow to check their resolution without needing to correct for factors introduced by the APTS chips and the SiPM. As both remained connected to the circuitry during this process, this was crosschecked by repeating the measurement with different chips and voltages applied, which yielded no different results.

The spectrum for the calculation of the timing resolution of the Pitch 10 Pixel 9, at $4.8V_{bb}$ can be seen in figure 3.5. Applying the process described in section 3.4 one can calculate an intrinsic time resolution of 0.11 ± 0.001 ns for the electronics.

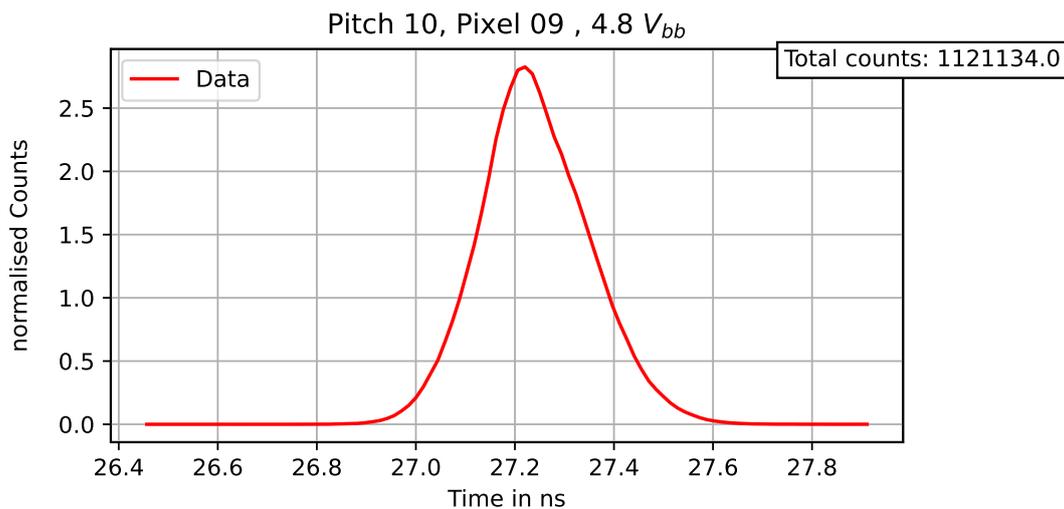


Figure 3.5: A typical spectrum used in the calculation of the electronics resolution of the system

3.3.2 The silicon photomultiplier

In order to compute the contribution σ_{SiPM} from equation 3.1, a simple simulation was completed. As the particle hits the plastic scintillator BCF-12 8000 photons are created per MeV of energy. Assuming full energy deposition of our β particle, about 4000 photons per β particle are expected. The photon emission probability rises for approximately 1ns and then decays back down to $\frac{1}{e}$ with a decay constant τ_{decay} of 3ns [32, p. 3]. Of these photons only 32% are collected by our silicon photomultiplier, which results in a total of 1280 photon hits, assuming no double hits on a single pixel. Each pixel of the 1 by 1 mm active area of the photomultiplier then emits a signal with a signal rise time τ_{signal} of approximately 110 ps [33, p. 2]. To model this process, at first the emission distribution was calculated from the above assumptions, resulting in equation 3.2 and subsequently normalised to the area between 0ns and 4ns.

$$p(t) = \begin{cases} e^t - 1, & \text{if } t \leq 1ns \\ (e - 1) \cdot e^{-\frac{t-1}{\tau_{decay}}}, & \text{if } t > 1ns \end{cases} \quad (3.2)$$

According to the probabilities of emission resulting from this distribution, 1280 samples, the number of photons measured, were taken. Each of those samples time coordinates was then assumed to be the peak position of a Gaussian signal with a σ equal to the signal rise time τ_{signal} .

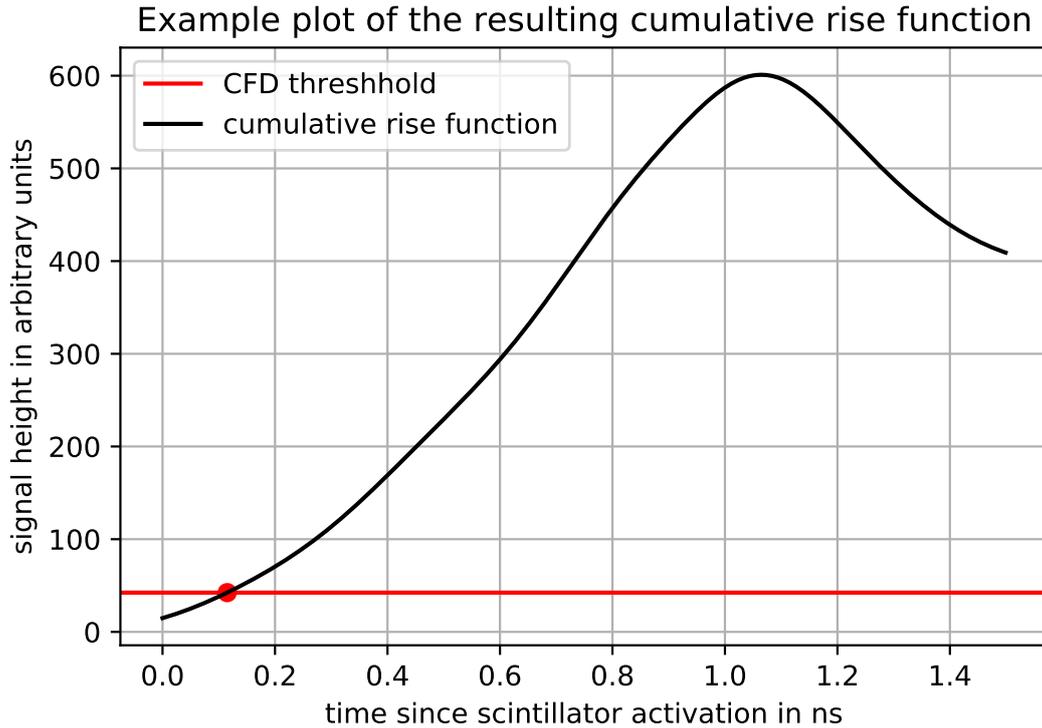


Figure 3.6: An example of the resulting simulated signal response of the SiPM

The resulting functions were then summed up in the area in between 0 ns and 1.5 ns, resulting in a spectrum like in figure 3.6. To get the fraction of the signal, at which it crosses the CFD noise

3 Experiment

threshold, this threshold was divided by the average signal height after amplification of $\approx 1V$. The resulting time coordinate of the crossing, was then taken as the minimum timing resolution of the SiPM. To account for statistical anomalies, this sampling process was repeated 1000 times and the average timing resolution was calculated. For the given assumptions this results in a time resolution of 99 ps for σ_{SiPM} .

3.4 Typical measurements and evaluation methods

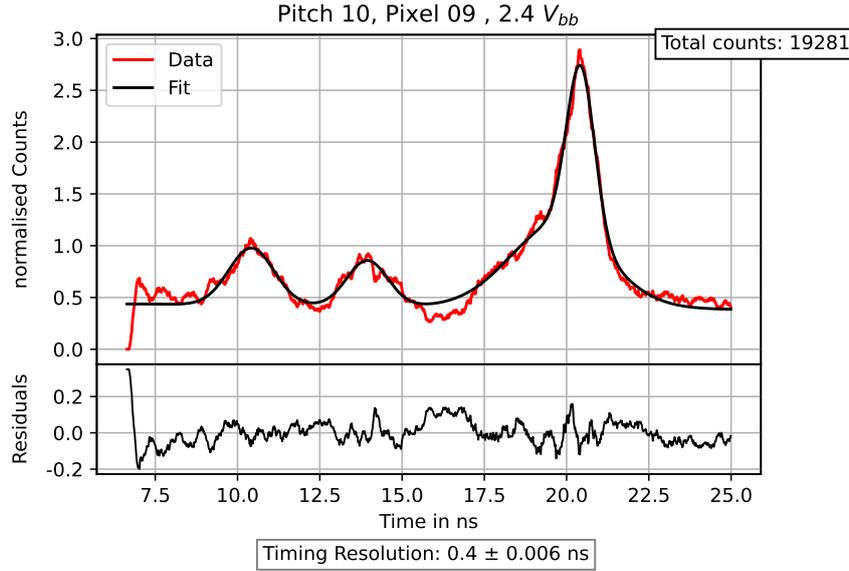


Figure 3.7: A typical spectrum measured to find the timing resolution of the system and corresponding fit curve

A typical spectrum taken at 2.4V V_{bb} can be seen in figure 3.7. As this setup is build to measure coincidences, all the peaks were assumed to be of Gaussian nature, resulting in the fit equation 3.3.

$$f(x) = A_1 \cdot e^{-\frac{1}{2} \cdot \frac{(x-\mu_1)^2}{\sigma_1^2}} + A_2 \cdot e^{-\frac{1}{2} \cdot \frac{(x-\mu_2)^2}{\sigma_2^2}} + A_3 \cdot e^{-\frac{1}{2} \cdot \frac{(x-\mu_3)^2}{\sigma_3^2}} + A_{main} \cdot e^{-\frac{1}{2} \cdot \frac{(x-\mu_{main})^2}{\sigma_{main}^2}} + a \cdot x + b \quad (3.3)$$

The spectrum consists of a main peak at around 18 ns and three smaller peaks to the left of it and a linear electronic noise background. These smaller side peaks increase in size and area contribution the lower the applied V_{bb} and the higher the pitch size measured, which is not a unexpected effect. Because peaks at lower delay time indicate either a earlier arriving SiPM signal or a later APTS signal. Whereas the parameter varied did only impact the APTS chips, the signs point to an intrinsic APTS effect. Taking a look at the varied parameters, these mainly impact the depletion region and especially the zero field region in between adjacent pixels. Lower V_{bb} reduces the strength of the lateral field, while the increased pitch size broadens the zero field region directly. Statistical accumulations visible in the spectrum, therefore imply a higher charge

3 Experiment

collection time, depended on a pattern in the depletion zones. One possible explanation for those peaks, is the hit's position on the pixel itself. A hit in or close to the zero field region creates charges that cannot be depleted in adequate time, creating a delayed signal to the left of the main peak.

Operating under this assumptions, the standard deviation of the main peak at 18 ns is interpreted as the best achievable timing resolution $\sigma_{measured}$ in equation 3.1. This approach holds for all applied V_{bb} except 0.0V, as can be seen in figure 3.8. At this voltage the contribution of the side peaks matches or even exceeds the contribution of the main peak at 18 ns, pointing to a not fully depleted n blanket. This is especially problematic for the side peak closest to the main peak, the one acting as a shoulder to the main peak for V_{bb} 1.2V to 4.8V. At 0.0V the short distance in between the two creates a large overlap of the two Gaussians, making resolving them mathematically impossible. Trying to fix the distances in between the two Gaussians resulted in no significant improvement.

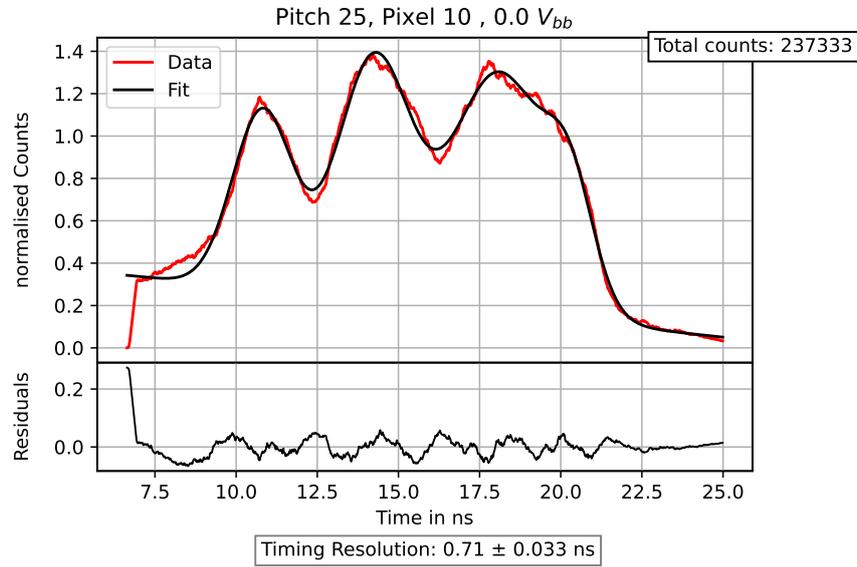


Figure 3.8: A typical spectrum for $V_{bb} = 0.0V$

3.5 Time Calibration

As the MCA software computes the pulse height of the incoming TAC signal in built-in bins and not in nanoseconds as needed, a time calibration had to be done. For that a pulser was introduced at the same position as can be seen in figure 3.4 and additionally a delay box was put in place in between the CFD of the SiPM and the TAC. The accurate tuning of the delay, this device makes possible, allows for calibrating the MCA bins to time conversion curve, assuming a linear conversion rate with an unknown offset. This offset was introduced to account for unknown, inbuilt delays of the system, to allow for a finetuning of the calibration. To account for possible effects of different pixels or V_{bb} , which may introduce an unknown effect into the system, it was again crosschecked with different chips. This yielded no significantly different results.

3 Experiment

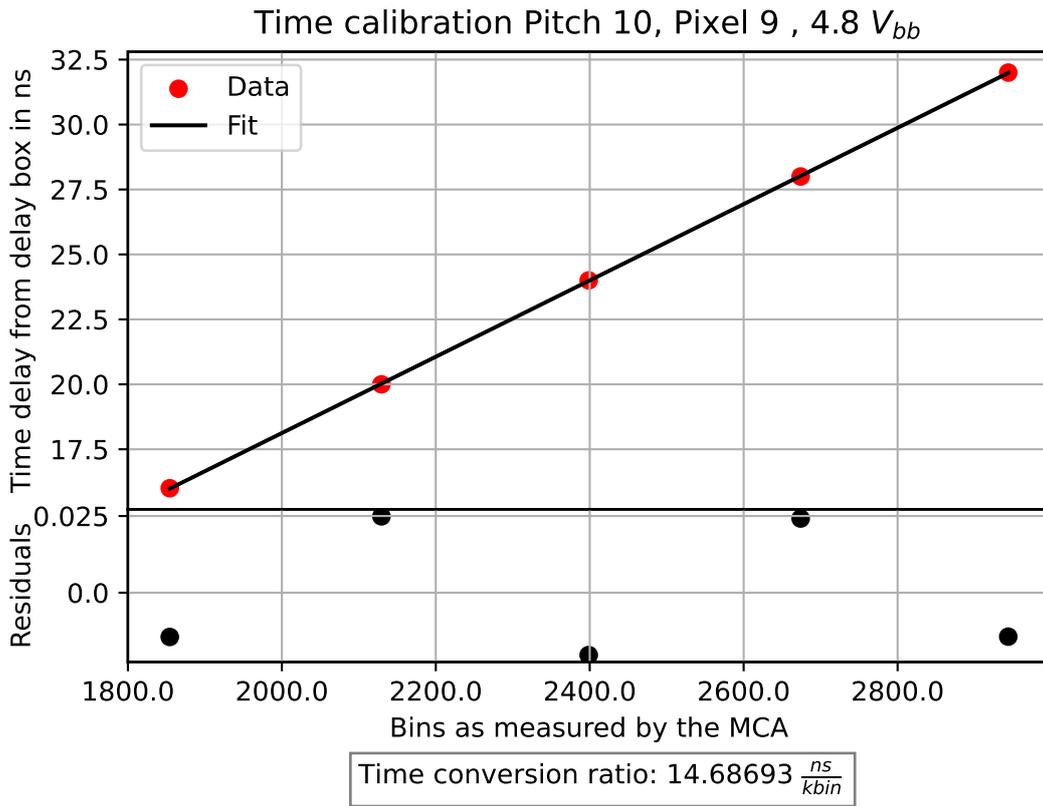
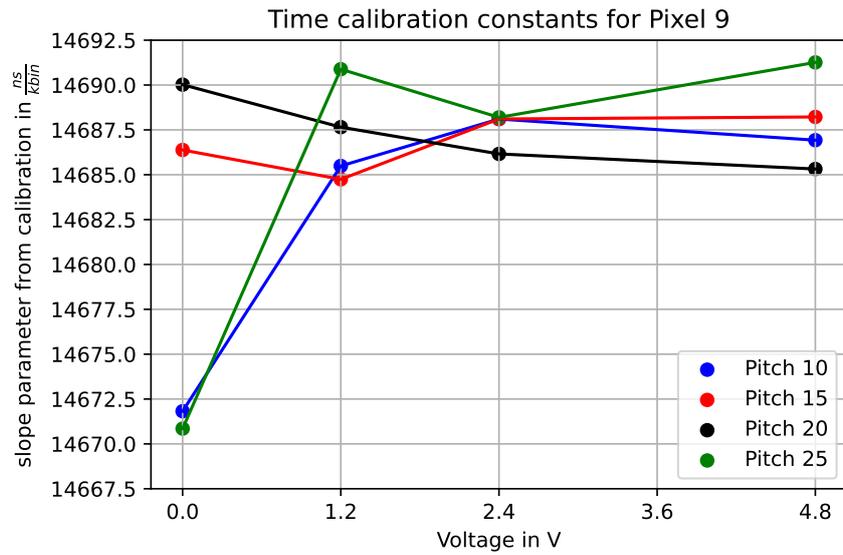


Figure 3.9: Time delay as a function of the MCA bins. The slope of the curve was used to compute the time conversion rate.

An example calibration curve can be seen in figure 3.9, with the resulting bins to time conversion ratio. The exact bin position was obtained as the peak position of a Gaussian with a linear background fitted to the spectra taken by the MCA. As approximately 1 million counts were taken per peak the statistical error of computing the peak position becomes insignificant and can be neglected. Furthermore, when taking a closer look at the residuals of this fit, it is noticeable that the errors on the parameter are in the order of magnitude of 10^{-9} , which is too small to significantly contribute to the further calculation.

This process was repeated for all the used pitch sizes and applied V_{bb} . The resulting conversion ratios can be seen in figures 3.10 and 3.11, as well as their exact values in tables 3.1 and 3.2, respectively. For further calculations the mean value of $14.68 \frac{ns}{kbin}$ was used. It is important to note that even though the curves imply a huge difference in between the different time calibration constants, this is only due to the axis scaling, and they are in fact quite similar and only differ by about $0.02 \frac{ns}{kbin}$.

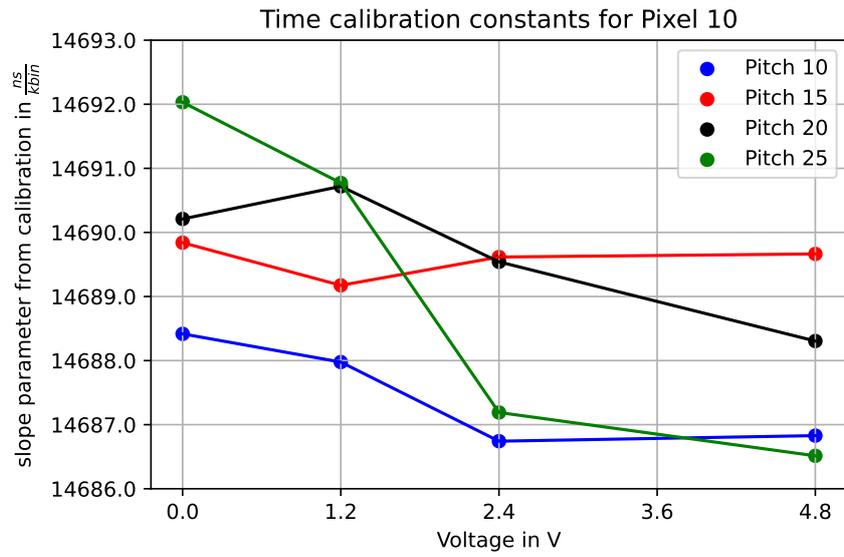
3 Experiment



Pitch	0.0V	1.2V	2.4V	4.8V
10	14.671822	14.685490	14.688105	14.686927
15	14.68638	14.684745	14.688108	14.688221
20	14.690021	14.687653	14.686161	14.68532
25	14.670852	14.690882	14.688197	14.69126

Figure 3.10 & Table 3.1: Time calibration constants in $\frac{ns}{kbin}$ for pixel 9

3 Experiment



Pitch	0.0V	1.2V	2.4V	4.8V
10	14.688417	14.687977	14.686742	14.686829
15	14.68984	14.689174	14.689616	14.689664
20	14.69021	14.690719	14.689541	14.688305
25	14.692031	14.690772	14.68719	14.686514

Figure 3.11 & Table 3.2: Time calibration constants in $\frac{ns}{kbin}$ for pixel 10

4 Evaluation of the timing resolution

In this chapter the results for the timing resolution of the APTS will be presented. It is crucial to emphasise, that the resolutions obtained, as a result of the data analysis method described in section 3.4, have to be interpreted as the best timing resolution achievable.

4.1 Trends for different voltages

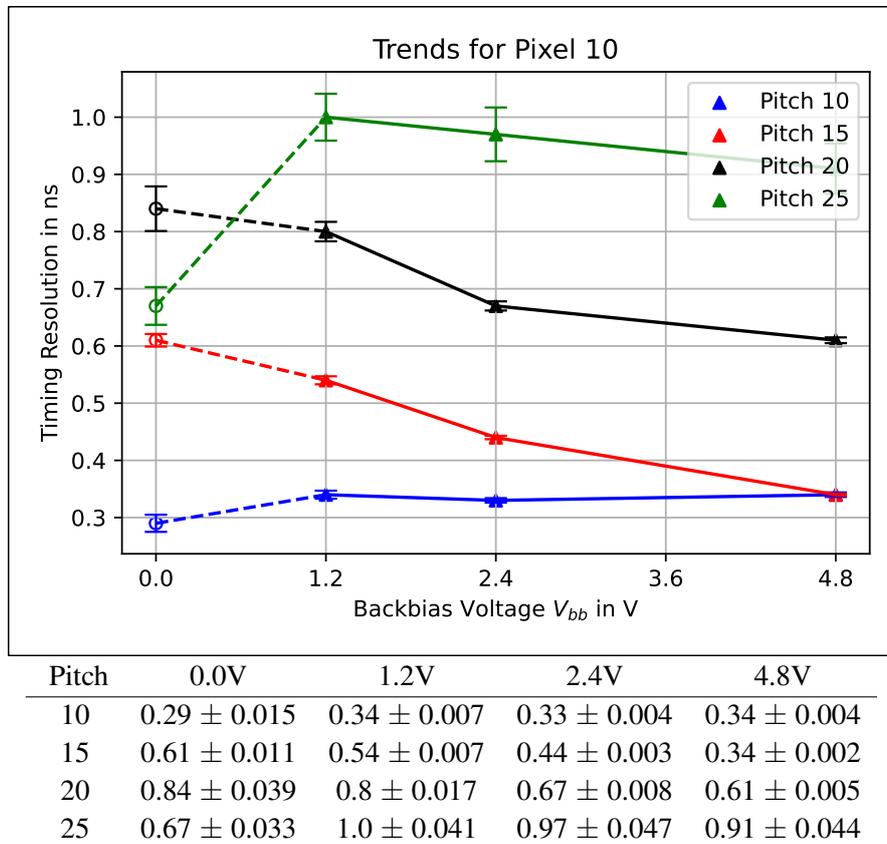


Figure 4.1 & Table 4.1: Timing Resolutions for the pixel 10 in ns

The calculated timing resolutions can be seen in the figures 4.1 and 4.2, their exact values can be found in the tables 4.1 and 4.2 respectively. Data points for V_{bb} 0.0V are marked with dashed lines as the fitting procedure does not hold for this high noise regime. Details can be seen in section 3.4. For this reason 0.0V data is only shown for completeness and will not be mentioned in further discussion.

4 Evaluation of the timing resolution

A general trend that can be observed for the pitch sizes 10 to 25 is that the timing resolution decreases with increased voltage. This effect is expected as for none of those pixel sizes the depletion zone is expected to cover the full n-blanket without any V_{bb} applied. Consequently, the decreasing efficiency of higher voltage applications is also expected. As previously discussed in section 2.1, when treating the n-well diode and the surrounding depletion zone as a spherical capacitor, the voltage U is directly proportional to the depletion radius r . As the pixel geometry itself is not spherical, at a certain point, the depletion radius r would exceed the pixel radius in some areas while still not covering the corners of the pixel region. This decreasing return on investment can be seen in the lower efficiency of higher voltage application.

4.2 Trends for different pixel sizes

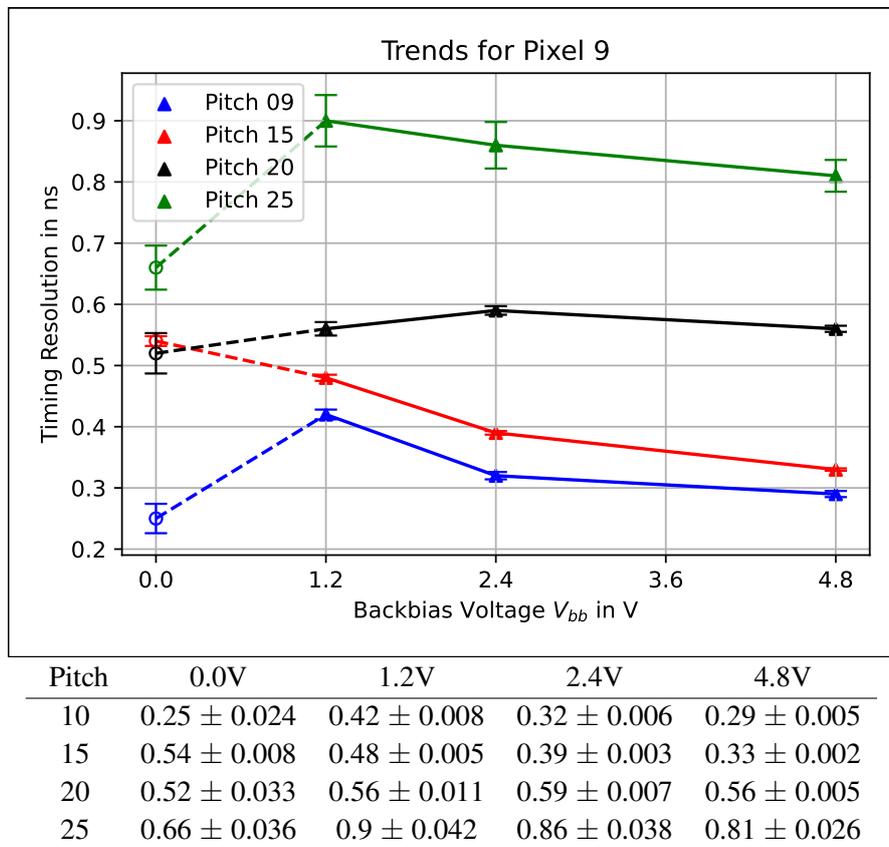


Figure 4.2 & Table 4.2: Timing resolutions for pixel number 9 in ns

Taking a look at the different pixel sizes in figures 4.1 and 4.2, one trend can immediately be noticed. Smaller pixel sizes directly correspond to lower timing resolution. This simple effect can be attributed to lower distances in between the charge created by the ionising radiation and the n-well diode. Assuming a similar charge carrier velocity for all pixels is a valid expectation as the pixels are made of the same material. The shorter distance directly translates into a shorter charge collection time. This in turn decreases the timing resolution, which leads to the effect observed.

5 Summary and Outlook

During the long shutdown 3 the LHC will undergo a major upgrade. It is planned to increase its luminosity by orders of magnitude. This development poses a significant challenge to the detector systems along its ring, especially regarding their radiation hardness and charge collection capabilities. For this reasons maintenance, refurbishment and upgrades of the existing infrastructure will be of utmost importance to ensure maximum performance. One of the systems undergoing major upgrades will be the ALICE detector. The Inner Tracking System will be upgraded to match the new requirements in radiation hardness, while simultaneously improving its position and tracking capabilities. To achieve that a new silicon pixel detector will be constructed. Key improvements will be made utilising 65nm CMOS technology, stitching and bending of large silicon wafers. Ensuring that the physics goals of the upgrade will be met, requires extensive testing of the new technologies. For this reason three new test structures have been commissioned, the CE65, the DPTS and the APTS. In this context, the goal of this work was to test the timing resolution of the new APTS chips. As simulations already showed the best possible performance for the modified with gap doping profile for the pixel detector, only chips of these type were examined. Their timing resolution was investigated at all possible different manufactured sizes, ranging from 10 μm to 25 μm and at different backbias voltages.

Timing resolutions of the APTS chips could be evaluated to lie in between 1.0ns and 0.29ns, depending on pixel size and V_{bb} applied. For smaller pixel sizes the timing resolution improves, the same happens for higher V_{bb} . An interesting effect visible when examining the V_{bb} is the saturation for higher voltages, pointing to a full depletion of the n-blanket. This poses a decisive improvement over its predecessor, the ALPIDE, with a timing resolution of only 2 μs to 4 μs . Significant improvements in the development of silicon pixel sensors open the door for a wide range of applications.

During this investigations another interesting effect was visible in the spectra of the timing resolution. Three side peaks were observed, increasing in area to levels comparable to the main peak, when the applied backbias voltage was decreased. A possible explanation offered for this effect is a decreased size of the depletion zone, resulting in slower depletion of the charges created on the border in between two pixels. While it was not possible to do this with the setup constructed for this study, future in-beam-experiments could focus ionising particles on different areas of a single pixel. This would allow to check aforementioned hypothesis and allow a study on the impact of hit position on charge collection and timing resolution.

List of Figures

1.1	Overall view of the LHC, including the ALICE, ATLAS, CMS and LHCb experiments [1]	2
1.2	Graphic showing the main upgrade points for the HL-LHC [4]	3
1.3	Graphic showing the ALICE detector systems, humans for scale [5]	4
1.4	Conceptual layout of the previous version of the inner tracking system ITS2 [7]	5
1.5	Schematics of IB (left) and OB (right) staves. Even though IB and OB staves have different geometries, both have the same core features [9, p. 13].	6
1.6	Azimuthal distribution of the material of layer 0 in terms of radiation length [8, p. 7]	7
1.7	The proposed layout of the IB of the new ITS3 utilising bent silicon chips and carbon foam for support [8, p. 10]	8
1.8	The proposed electronic readout and power supply endcap for the ITS3 [8, p. 11]	8
2.1	Schematic working principle of a MAPS-epi sensor [11, p. 10]	10
2.2	Scheme of a deep p-well shielding. The n-well contains the signal processing units [11, p. 10]	11
2.3	Scheme of ALPIDE sensor doping profile, with deep P-well to shield the signal processing electronics [15, p. 2]	13
2.4	TCAD Simulation: electric field for the standard process, applied V_{bb} of 4.8 V [18, p. 4]	14
2.5	A low dose n-type blanket is introduced to improve performance [14, p. 4] . . .	14
2.6	TCAD Simulation: electric field for the modified process, applied V_{bb} of 4.8 V [18, p. 4]	15
2.7	A gap in the low dose n-type blanket is introduced, creating a lateral field [20, p. 7]	16
2.8	TCAD Simulation: electric field for the modified process with gap, applied V_{bb} of 4.8 V [18, p. 4]	16
2.9	All available test structures, the APTS is marked in red[21, p. 5]	17
2.10	Pixel numeration of the APTS inner 4 by 4 matrix, used pixels in green	17
3.1	Picture of the housing of the setup together with the readout electronics. From top to bottom: DAQ board, proximity card and breakout board, green cable for SiPM signal, frontal cable out of breakout board for APTS signal	19
3.2	Scheme of the inside of the housing with distances in mm	20
3.3	Circuitry used to measure the timing resolution	21
3.4	Circuit scheme of the configuration used to measure the internal timing resolution	22
3.5	A typical spectrum used for the calculation of the electronics resolution of the system	22
3.6	An example of the resulting simulated signal response of the SiPM	23
3.7	A typical spectrum measured to find the timing resolution of the system and corresponding fit curve	24

List of Figures

3.8	A typical spectrum for $V_{bb} = 0.0V$	25
3.9	Time delay as a function of the MCA bins. The slope of the curve was used to compute the time conversion rate.	26
3.10	Time calibration constants in $\frac{ns}{kbin}$ for pixel 9	27
3.11	Time calibration constants in $\frac{ns}{kbin}$ for pixel 10	28
4.1	Timing Resolutions for the pixel 10 in ns	29
4.2	Timing resolutions for pixel number 9 in ns	30

List of Tables

3.1	Time calibration constants in $\frac{ns}{kbin}$ for pixel 9	27
3.2	Time calibration constants in $\frac{ns}{kbin}$ for pixel 10	28
4.1	Timing Resolutions for the pixel 10 in ns	29
4.2	Timing resolutions for pixel number 9 in ns	30

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