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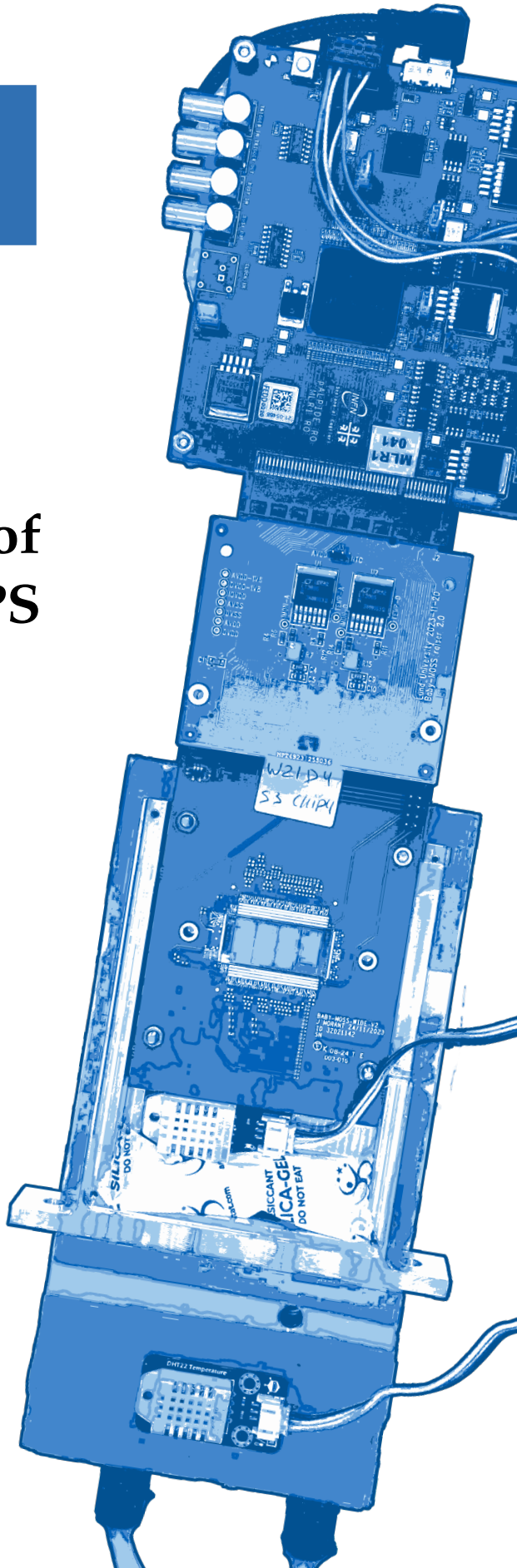
Bachelor's Thesis

Studying the Impact of Temperature on MAPS Detector Performance

Lena Kirchner



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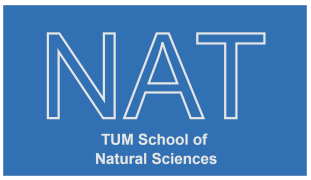

Studying the Impact of Temperature on MAPS Detector Performance

Untersuchung des Einflusses von Temperatur auf die Leistung von MAPS Detektoren

Bachelor's Thesis

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Date: September 16, 2024

I confirm that the results presented in this bachelor's thesis is my own work and I have documented all sources and materials used.

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Munich, September 16, 2024 Lena Kirchner

Abstract

Future High Energy Physics experiments are anticipated to heavily rely on Monolithic Active Pixel Sensors (MAPS) utilizing CMOS technology. As the performance requirements for these detectors continue to grow, managing effective cooling becomes a critical challenge. Understanding how temperature affects detector performance is therefore essential.

This thesis explores the influence of temperature on the performance of prototypes developed as part of the ALICE ITS3 upgrade. The study focuses on three different sensors: APTS, DPTS, and BabyMOSS, including two irradiated samples of the APTS, offering the opportunity for investigating the sensor performance at different stages of signal processing. In the conducted experiments, the detectors were operated across a temperature range of 5°C to 45°C. For this purpose, a new test setup was constructed to create a stable, temperature-controlled environment, enabling systematic investigations.

Temperature dependent parameters that were examined are the operating range and the waveform of the analogue signal after pulsing of the APTS. For the DPTS and the BabyMOSS, the threshold, noise and the fake hit rate were studied. Additionally, the DPTS was pulsed in order to perform a waveform analysis of the digital output, as well as the encoding timing parameter were investigated.

The results reveal that while the non-irradiated prototypes show performance variations with temperature changes, they remain functional throughout the tested temperature range. In contrast, the irradiated APTS prototypes exhibited significant performance degradation beyond 25°C, leading to their operational failure. These findings provide important insights into the thermal sensitivities of these prototype sensors and highlight the need for careful temperature management in the development and deployment of future MAPS based detectors.

Contents

1. Introduction

1.1. The Large Hadron Collider

The Large Hadron Collider (LHC) is part of CERN (*Conseil Européen pour la Recherche Nucléaire*) and the most powerful and largest particle accelerator in the world.[1] Since it became operational on the 10th of September in 2008, the LHC's biggest achievement so far is the discovery of the Higgs boson, which was announced on the 4th of July 2012. It is situated in a in a tunnel 100 m underground close to Geneva, Switzerland, and has a circumference of 27 km. The CERN accelerator complex operates as a series of progressively advanced machines, each designed to accelerate particle beams to higher energies than the previous one. In this setup, each machine boosts the energy of the particle beam before passing it on to the next machine in the sequence. The LHC represents the culmination of this process, where particle beams reach their peak energies.[2]

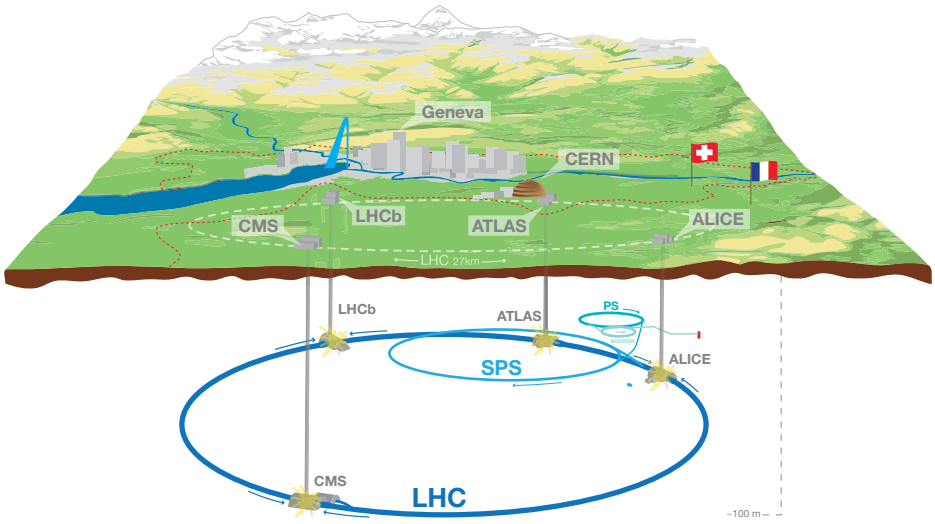


Figure 1.1.: Overall view of the LHC, including the ALICE, ATLAS, CMS and LHCb experiments.[3]

In the LHC, two beams of protons or ions are accelerated to speeds close to that of light and then directed to collide. These beams move in opposite directions within two separate beam pipes, which are kept under ultrahigh vacuum conditions. The beams are guided around the circular accelerator by a robust magnetic field generated by superconducting electromagnets. Superconducting materials are chosen for their ability to conduct electricity without resistance when cooled below a certain temperature. Consequently, the LHC's electromagnets are chilled to an extremely low temperature of $-271.3°C$ (1.9K), which is colder than the temperature of outer space. This cooling is facilitated by an extensive liquid helium distribution system, which ensures the magnets remain at the required temperature and supports other necessary operations. Each year, for a specific period, the LHC conducts collisions between lead ions, which simulate the conditions that prevailed shortly after the Big Bang. These high-energy collisions result in the formation of quark-gluon plasma, a transient state of extremely hot and dense matter. This provides a valuable opportunity for experiments to investigate the fundamental characteristics of matter under such extreme conditions.

The beams collide at four points around the accelerator[2], which is where the following detectors are situated as seen in figure 1.1.

ALICE: Detector focused on heavy-ion collisions.[4]

ATLAS: General purpose detector, explores a diverse array of physics, like the Higgs boson, extra dimensions or dark matter candidates.[5]

CMS: General purpose detector, shares the same scientific objectives as ATLAS, but employs distinct technical approaches and a different magnet system design. [6]

LHCb: Focuses on examining the subtle differences between matter and antimatter by inspecting beauty quarks, has a series of subdetectors to primarily detect forward particles.[7]

1.2. The ALICE Detector

ALICE, which is short for *A Large Ion Collider Experiment*, was built to investigate the characteristics of the quark-gluon plasma in heavy-ion collisions such as Pb-Pb. It consists of a range of specialized detectors, each tailored to study specific properties of the particles generated in the collisions. Amongst these are the Inner Tracking System (ITS), Electromagnetic Calorimeter (EMCal), Time-of-Flight (TOF) and the Time Projection Chamber (TPC).[4] Figure 1.2 gives a schematic overview of the ALICE experiment and its subdetectors.

1.2.1. The Inner Tracking System

The currently used Inner Tracking System (ITS2) was installed during the LHC Long Shutdown 2 (2019-2021), utilizes the ALPIDE sensor and is the largest-scale implementation of Monolithic Active Pixel Sensors (MAPS) in a high-energy physics experiment.[8]

It can be grouped into two sections, the inner barrel (IB), which arranged in three layers and the outer barrel (OB) consisting of two double layers, as shown in figure 1.3a.

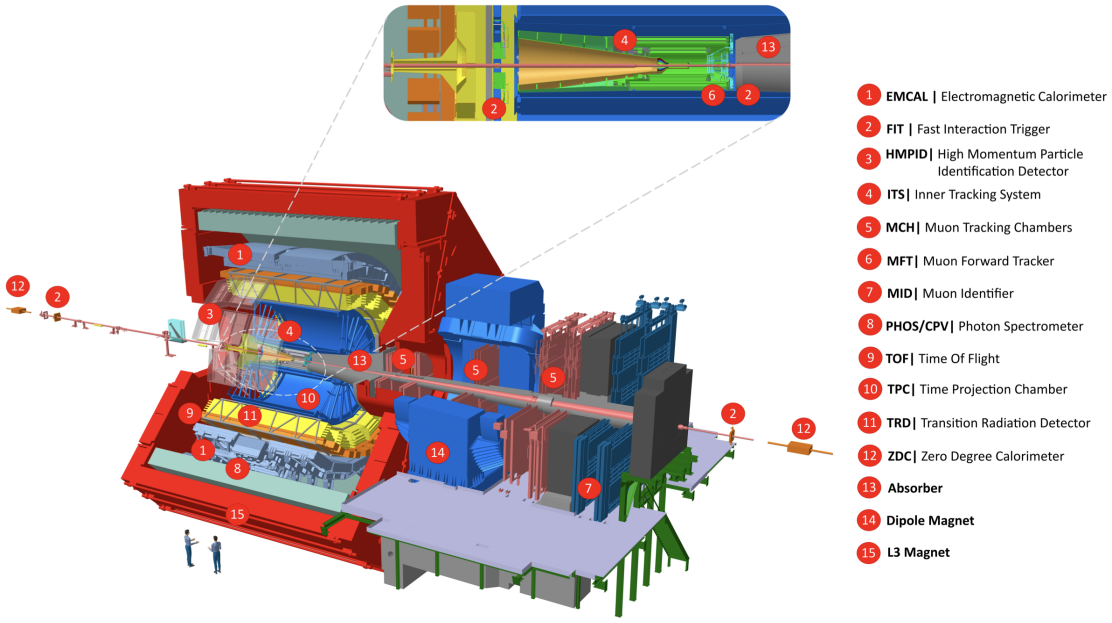
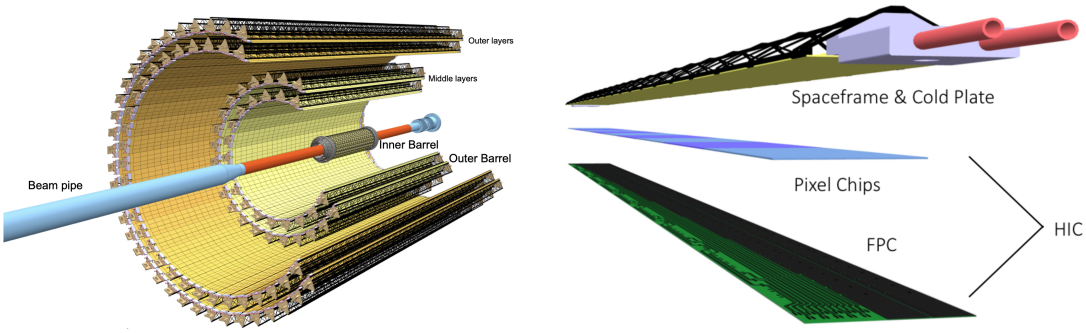


Figure 1.2.: Overall view of the ALICE detector.[8]



(a) Schematic view of the ITS2 subdetector.[8] (b) Schematic of the staves of the ITS2 IB.[9]

Figure 1.3.: Schematics of the ITS2.

The radial positioning of each layer was fine-tuned to enhance performance, focusing on pointing resolution, transverse momentum (p_T) accuracy, and tracking efficiency in the highly-dense track conditions of Pb–Pb collisions, with the layer closest to the beam being situated just 22.4 mm away from the interaction point. Every one of these layers are composed of so-called staves, shown in figure 1.3b, which consist of the following materials[8]:

Hybrid Integrated Circuit: An assembly consisting of a polyimide Flexible Printed Circuit onto which some passive components along with the pixel chips are bonded.

Space Frame: A truss-like carbon fiber structure provides mechanical support and the required stiffness to mount HICs on cold plates.

Cold Plate: A thermally conductive carbon fiber sheet with embedded polyimide

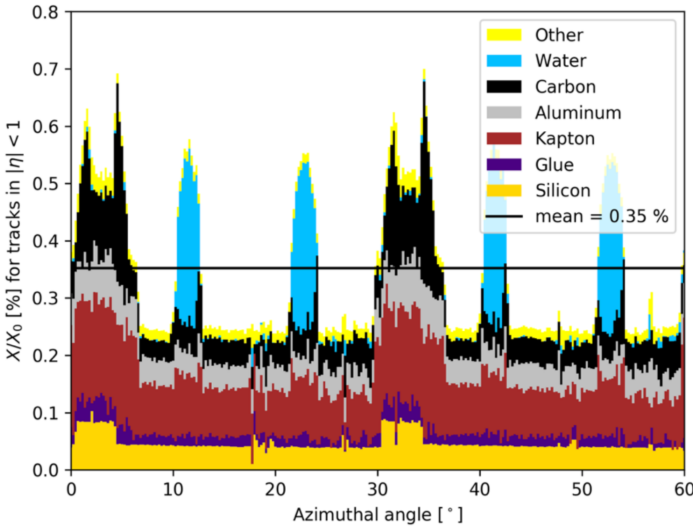


Figure 1.4.: Azimuthal distribution of the material budget of the innermost layer with regard to radiation length.[9]

cooling pipes is integrated into the space frame for inner barrel staves and attached to the frame for outer barrel staves.[8] It is in thermal contact with the pixel chips in order to remove the generated heat.

In order to guarantee hermeticity, adjacent staves are partially overlapping, which can be seen in Figure 1.4, where the highest peaks are equal to these locations. The blue peaks represent the water in the polyimide cooling pipes that are embedded in the Cold Plate. Maintaining a low average value of 0.35 %X_0 is essential for achieving high impact parameter accuracy at low transverse momentum, further enhancing the system's overall performance.[9] X_0 is called the radiation length of a material and corresponds to the average distance in cm required to reduce an electron's energy by a factor of $\frac{1}{e}$[10]. It can also be observed, that the silicon sensor itself contributes only a small factor to the total material budget—15 % to be precise—and it is the only component that must be in the detector's acceptance. Most of the increase in the material budget is because of the electrical substrate, where Kapton is used for electrical insulation and glue for bonding, along with the other wiring components, which together account for 50 % of the total. The rest is due to the Space Frame (15 %) providing stability and the cooling circuit (20 %). So to decrease the material budget and thereby reduce the amount of multiple scattering, it is clear that the next focus must be on minimizing the electrical, mechanical, and cooling materials.[9]

One potential solution to reduce the material from the cooling circuit is to replace the current water cooling system with an air flow, that has to be low-speed, to cool the innermost ITS layers. In the testing for the ITS2, it was already shown that this is indeed a possible option for sensors with a power density below 20 $\frac{\mathrm{mW}}{\mathrm{m}^2}$. The currently used ALPIDE chip has a power density of around 40 $\frac{\mathrm{mW}}{\mathrm{m}^2}$, but most of that is dissipated by the digital interface circuitry and the high-speed output data links. The pixel matrix itself only has a power density of 7 $\frac{\mathrm{mW}}{\mathrm{m}^2}$, which is well below the limit of 20 $\frac{\mathrm{mW}}{\mathrm{m}^2}$.[9]

With the help of a new technology called stitching, it is possible to construct a

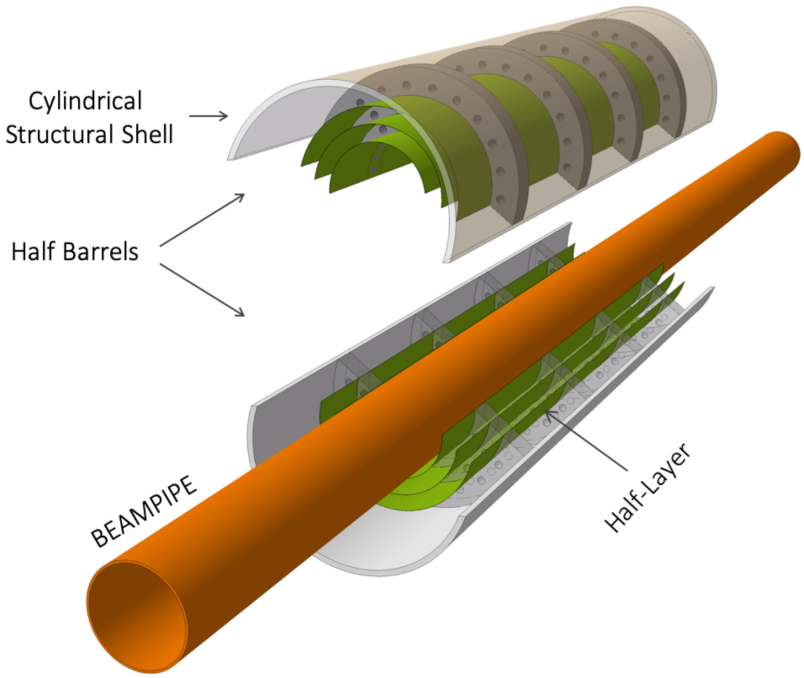


Figure 1.5.: Layout of the planned ITS3 Inner Barrel, showing the half-barrels mounted around the beampipe.[9]

wafer-scale sensor that is the size of a half-layer of the inner barrel. Additionally, the sensor will be thinned down to only $20 - 40\,\mu m$, meaning it is possible to bend and still be able to operate the chip, which opens up the option for silicon-only cylindrical layers.[9]

The upcoming ITS3 will utilize this technology, and it will be composed of two barrels, the Inner Barrel and the Outer Barrel, just like in the ITS2. While the OB will remain in use from the ITS2, the IB will be replaced entirely. It will feature two half barrels, each made up of three layers installed around the beampipe, as shown in Figure 1.5. Each of those layers will be composed of a single large pixel chip, bent into a cylindrical shape to ensure high coverage.[9]

In between those layers, there are carbon foam half-rings improving the cooling by enlarging the surface area that is in direct contact with the airflow, while also maintaining a low material budget. The outermost layer is mounted to a Cylindrical Structural Shell (CYSS), which is enhancing the mechanical stability[11], as well as to the End-Wheels. Both the CYSS and the End-Wheels are made of Carbon Fibre Reinforced Plastic and are connected. Since the half-layers consist solely of the silicon pixel, all peripheral components and interface pads are located on one edge. Here, they connect to a flexible printed circuit that extends through the End-Wheel to a patch panel a few centimeters away, where all data and power cables are situated.[9]

Due to this design, the material budget is significantly reduced, resulting in an average of 0.09% X_0 for tracks with a pseudorapidity $|\eta| < 1$ in the innermost layer.[11] In Figure 1.6 this is shown as a function of the azimuthal angle φ and η.

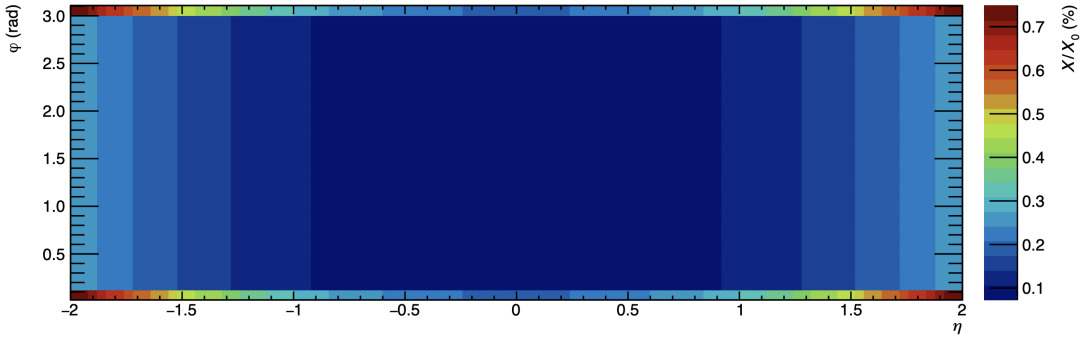


Figure 1.6.: Estimated material budget of half-layer element 0 for particles originating from the interaction point, shown as a function of the azimuthal angle φ and the pseudorapidity η.[11]

1.3. Monolithic Active Pixel Sensors

MAPS, an acronym for *Monolithic Active Pixel Sensors*, are pixel detectors integrating CMOS (*Complementary Metal-Oxide-Semiconductor*) electronics and charge collection into a single, unified device. Commercial technologies usually use low-ohmic, low-cost substrate wafers, onto which an epitaxial silicon layer is grown. The doping profile and conductivity type of the epi-layer can be adjusted independently of the substrate, allowing it to be manufactured more cost-effectively, with higher purity, and greater resistivity than the substrate. In Figure 1.7, the working principle of a MAPS detector is shown. The CMOS wafer's substrate is not depleted, and there is essentially no directed electric field in the epi-layer. Electrons generated by incoming radiation within the epi-layer mostly reach an n^+-doped region, which serves as the collecting electrode, primarily through diffusion. In CMOS technology, this is achieved with an N-well. The design limits the use of PMOS transistors within the pixel cell because they need to be embedded in another N-well, which is a competition to the N-well collection diode. As a result, complex CMOS technology using NMOS and PMOS transistors must be placed outside the active pixel area. To incorporate PMOS transistors within the active area, deep well options are needed, such as a deep P-well that shields the N-well and prevents it from competing with the collection diode.[12]

Charge collection via diffusion is generally only fully effective when the charge is deposited directly at the collecting electrode, where a depletion region is present nearby. Since there is no drift field, charge collection through diffusion is relatively slow and inefficient, taking approximately 100 ns. This means the deposited charge is minimal, requiring the noise of the readout electronics to be very low to maintain an appropriate Signal-to-Noise Ratio.[12]

1.3.1. APTS

The APTS, which is short for *Analog Pixel Test Structure*, was produced in the TPSCo CMOS 65nm ISC technology and is a 1.5 mm $\times$ 1.5 mm sensor that holds a matrix of 4×4 pixels. Every pixel has its own analog output, which is buffered and linked to an

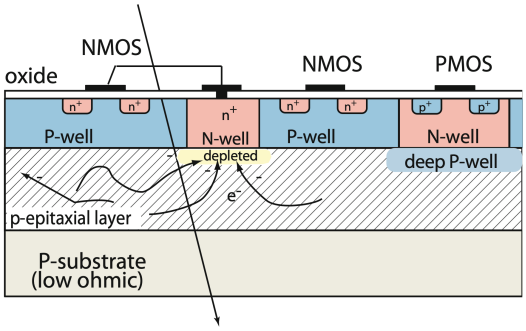
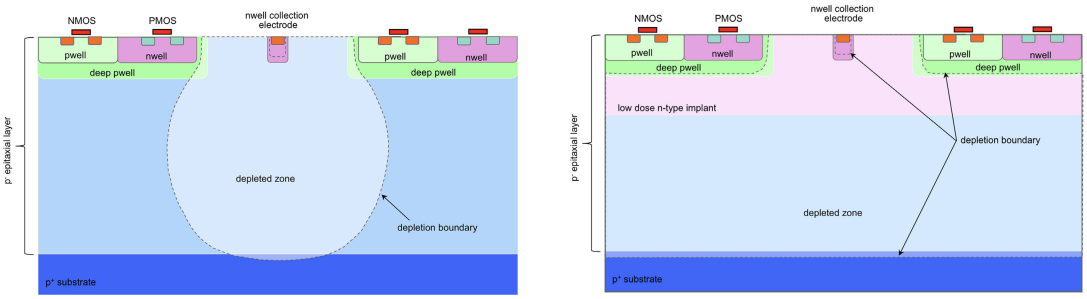


Figure 1.7.: Working principle of a MAPS detector.[12]



(a) Standard process[13]

(b) Modified process[13]

Figure 1.8.: Schematic of the different types of the APTS.

output pad, ensuring complete access to the signal's time evolution. To reduce electric field distortion, a ring of dummy pixels encircles the matrix of these 16 pixels. The chip was fabricated with four varying pixel sizes, also known as pixel pitches: 10, 15, 20, and 25 µm. However, only the 15 µm pitch was used for the experiments in the following work. There are three distinct designs for the APTS that were produced for the testing.[15]

The standard process, shown in Figure 1.8a, has a design related to the one used at the ALPIDE sensor. It incorporates a collection electrode, formed by n-well diffusion on a high-resistivity p-type epitaxial layer, which is grown over a low-resistivity p-type

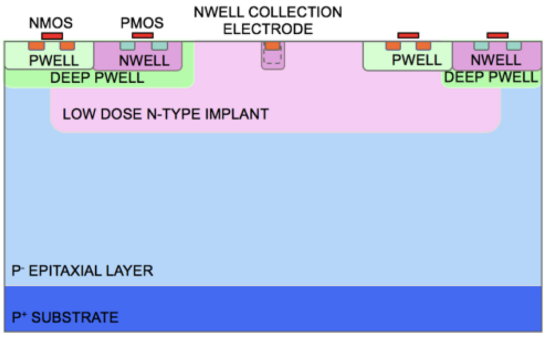
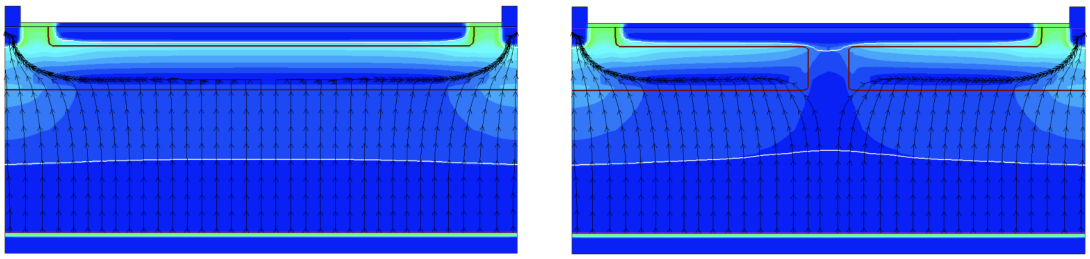


Figure 1.9.: Modified with gap[14]

substrate. The in-pixel circuits are located outside the collection electrode and housed within a deep p-well. This deep p-well isolates the n-wells in the circuitry from the epitaxial layer, preventing them from collecting charge and enabling the implementation of full CMOS circuitry. By this, a depleted region that has a balloon like shape is created, similar to the one of the ALPIDE sensor. It doesn't expand to the edges of the pixel, resulting in slower charge collection, as it occurs through diffusion rather than drift outside the depleted region.[15]

To counter this effect and extend the depleted region to cover nearly the full pixel even at $V_{BB} = 0\,\text{V}$, a deep, low-dose n-type implant is added beneath the entire pixel area, as shown in Figure 1.8b. To fully deplete the epitaxial layer, only a small back bias is required. This approach, known as the modified process, facilitates charge collection through drift.[13]

The third variant, called the "modified with gap", involves adding a 2.5 µm gap between two collection diodes in the n-type implant to increase the lateral electric field. This reduces charge sharing between pixels, since the zero-field region gets decreased, as illustrated in Figure 1.10. This causes a larger portion of the charge being collected by a single pixel, which in turn increases the Signal-to-Noise Ratio $\left(\frac{S}{N}\right)$, offering greater operational margins.[15]



(a) (b)

Figure 1.10.: Field lines of the **(a)** modified process and the **(b)** modified with gap design.[16]

The APTS pixel readout chain features both in-pixel and peripheral components, with the sensor represented by diode D0. The collection electrode is managed by a constant current mechanism, with the current source I_{RESET} compensating for leakage and resetting the pixel after a signal is detected. The in-pixel circuitry includes two source-follower stages: a PMOS follower (I_{biasp} and M2) and an NMOS follower (M3 and I_{biasn}). This design minimizes the capacitive load on the collection electrode. An additional pair of source-follower stages in the peripheral circuit buffers the signal from each pixel and sends it to an external ADC (*Analogue-to-Digital Converter*). A pulsing circuit allows for charge injection into the collection electrode via a capacitor ($C_{inj} = 242\,\text{aF}$) when triggered. The injected charge amount can be adjusted using the voltage setting V_h.[15]

For the following experiments, three different chips were used, with their properties listed in Table 1.1. Additionally, the chips AF15P_W22B11 and AF15P_W22B15 were often referred to as "Irr14" and "Irr15" based on their irradiation levels.

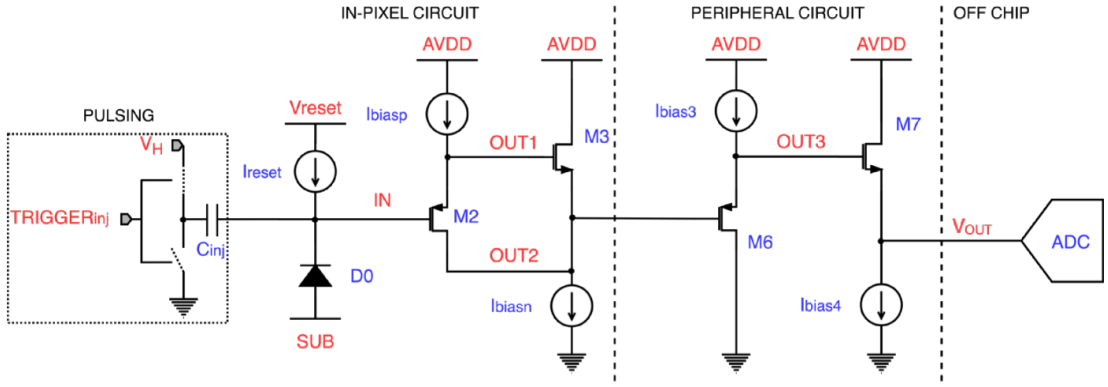


Figure 1.11.: Schematic of the front-end chain of the APTS.[15]

Table 1.1.: APTS used in the experiments.

ID	Readout	Design	Pixel Pitch [µm]	Irradiation
AF15P_W22B11	source follower	modified with gap	15	1e14
AF15P_W22B15	source follower	modified with gap	15	1e15
AF15P_W22B19	source follower	modified with gap	15	none

1.3.2. DPTS

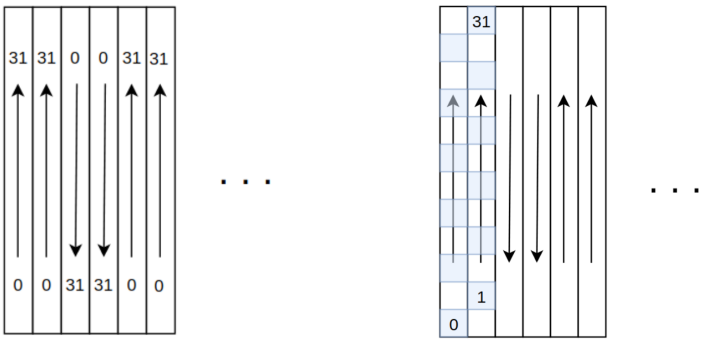
The DPTS (*Digital Pixel Test Structure*) was also produced in the TPSCo CMOS 65nm ISC technology, like the APTS. It was fabricated with the previously mentioned modified with gap process and includes a 32×32 pixel matrix with a 15 µm pitch size. The chip's dimensions are 1.5 mm $\times$ 1.5 mm. In the pixel, the signal gets amplified, shaped and discriminated. The main difference is that all 1024 pixels are read out simultaneously with one digital output line and the position of the pixel is time-encoded.[17]

There are 3 different kinds of chips which are characterized by using a different pixel mapping. The DPTS in the base version, which can be recognized by the "O" in the chip ID, is shown in Figure 1.12a. From a digital standpoint, the matrix organizes its pixels into columns, each assigned a group ID (GID) from 0 to 31, arranged from left to right. Within each column, pixels are given a pixel ID (PID) that ranges from 0 to 31. The PID sequence is inverted every two columns, as if the column were flipped vertically, starting from the bottom-left corner of the matrix. This vertical flipping is implemented to ensure a single output for all columns while minimizing the risk of readout collisions due to charge sharing along the horizontal axis. Instead of arbitrating charge sharing, the system processes all activated pixels and delays transmissions to prevent output collisions.[18]

The other two variants both make use of the following approach called column cross connect in order to minimize charge sharing in the vertical direction. They can be recognized by the "X" and "S" in their chip ID, with the difference between them being that the DPTS-S additionally has the DVSS and AVSS shorted. The discriminator outputs of two pixels in a column pair are switched at every other vertical position,

making the pixels appear swapped in the digital readout. However, this swap does not change their addressing in the slow control system for pulsing and masking. For instance, all the blue pixels in Figure 1.12b are part of group 0 in the matrix from a digital perspective. However, when manually pulsing those pixels, pixel 1 in the image is addressed as col = 1, row = 30.[18]

In this work, non-irradiated chips with both the basic encoding and the cross-connect encoding were used, their exact IDs are listed in Table 1.2.



(a) DPTS-O (b) DPTS-X

Figure 1.12.: Pixel mapping scheme of the **(a)** DPTS base version and the **(b)** DPTS-X column cross connect variant.[18]

Table 1.2.: DPTS used in the experiments.

ID	Variant	Irradiation
DPTSXW22B30	column cross connect	none
DPTSOW22B54	base version	none

After pulsing a pixel, its digital readout circuitry is triggered, and the signal is time-encoded as follows. As illustrated in Figure 1.13, the first pulse always has the same duration T_H, to ensure a minimal pulse length. To decode the pixel's position within the group or column (PID), the time difference between the first two rising edges is taken. This can be expressed by[19]

$$T_{PID} = T_H + \delta_P \cdot PID \tag{1.1}$$

where δ_P is a fixed delay of the XNOR gates in the chain. Next, the position of the column (GID) is encoded with the second pulse. The T_{PID} pulse is sent to a predefined

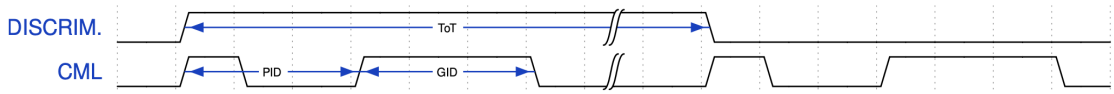


Figure 1.13.: DPTS encoding scheme of the hit position. In this case, PID and GID correspond to T_{PID} and T_{GID}.[17]

delay T_0, and then split. One part is sent through a line of delays δ_G similar to the PID encoding. The output of the GID chain is then fed into an OR logic gate along with the non-delayed signal, resulting in a pulse stretcher. In summary, the delay can be calculated by[19]

$$T_{GID} = T_0 + \delta_G \cdot GID \tag{1.2}$$

When the discriminator asserts and then deasserts, it generates two sets of pulses that define the time interval during which the front-end pulse remains above the threshold, known as the Time-over-Threshold (ToT). The front end is designed so that the pulse length increases with the input signal, allowing the ToT to reflect the amount of collected or injected charge. To encode this ToT interval, the same coordinate sequence is retransmitted when the comparator output drops back to zero, effectively capturing the duration for which the signal exceeded the threshold.[17, 19]

Since the delays are based on CMOS logic gates, they are sensitive to temperature, this is why the nominal timing parameters (see Table1.3) are simulated for $T = 27°C$.[19] To further characterize this temperature dependent time propagation, the average mobility of the electrons in non-polar semiconductors, like silicon or germanium, is proportional to $T^{-\frac{3}{2}}$[20], more exactly

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-\frac{3}{2}} \tag{1.3}$$

with a reference mobility $\mu(T_0)$ at a fixed temperature of T_0.[21] The propagation delay or time delay τ_P is proportional to

$$\tau_P \propto \frac{C_{out} V_{dd}}{\mu(T)(V_{dd} - V_T(T))} \propto T^{\frac{3}{2}} \tag{1.4}$$

and thus proportional to $T^{\frac{3}{2}}$, with the drain voltage V_{dd}, V_T the threshold voltage and C_{out} a capacitance.This means, if the temperature increases, the CMOS logic gates will be slower and since T_{PID} and T_{GID} are are realized with those gates, the timing performance will decrease.[22]

Table 1.3.: Simulated timing parameters of the DPTS.[19]

Parameter	T_0	T_H	δ_P	δ_G
Value [ns]	≈ 1	≈ 4.4	≈ 0.15	≈ 0.15

In Figure 1.14, the schematic front-end circuit of a DPTS is shown. It is controlled by six externally generated parameters, two are voltages (V_{casb} and V_{casn}) and four of them are currents (I_{bias}, I_{biasn}, I_{RESET} and I_{db}). The front end is built around a high-gain cascoded inverting amplifier that requires direct feedback to establish its operating point. This feedback is provided by the V_{casb} transistor (M6) in combination with the I_{RESET} current source (M5), ensuring that the current through the V_{casb} transistor equals I_{RESET} minus any leakage current, thus correctly setting the collection electrode's voltage. When charge accumulates on the collection diode, the amplifier output causes a positive voltage shift, turning off the V_{casb} transistor and resetting the collection diode with a constant current, resulting in nearly linear Time-over-Threshold (ToT)

behavior.[17] The high-gain amplifier output then feeds into a common-source stage,

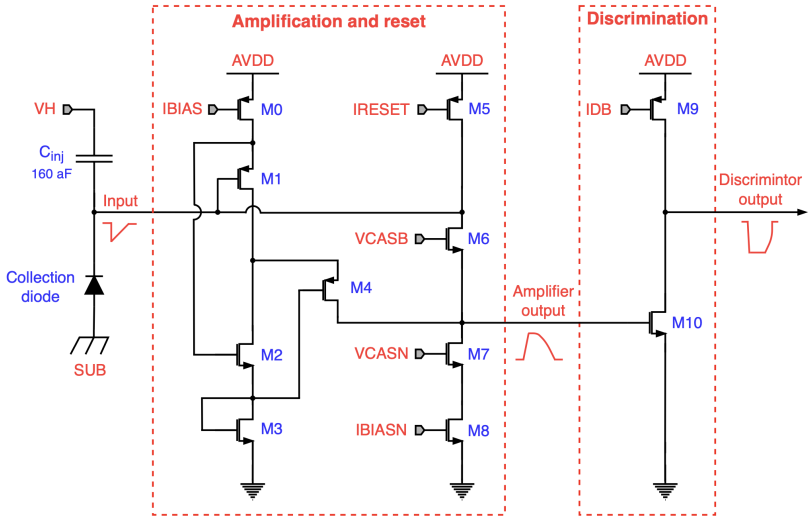


Figure 1.14.: Schematic of the front-end chain of the DPTS.[17]

where the signal is converted into a digital rail-to-rail signal once the amplifier output overcomes a threshold. The I_{biasn} current source (M8) balances the amplifier's output, operating at one-tenth of the I_{bias} current. V_{casn} (M7) is used to further fine-tune the amplifier's operating margin.[17]

NMOS transistors are influenced by the reverse bias applied to the sensor, requiring biases like V_{casb} and V_{casn} to be adjusted accordingly. Steady-state power consumption is primarily determined by the I_{bias} current, with the reset current being significantly lower, and the discriminator branch current only flowing when M10 is active.[17]

The pixel also includes test circuitry capable of injecting charge into the collection electrode through a 160 aF capacitor. The injected charge amount is controlled by an external voltage reference, V_h, and the injection is triggered by the TRG signal via an interface pad.[17]

1.3.3. BabyMOSS

The BabyMOSS sensor is based on the MOSS (*Monolithic Stitched Sensor*), which is a 6.7 megapixel sensor, measuring $1.4 \times 25.9\,\mathrm{cm}^2$ making it the largest prototype of the ER1. It consists of ten RSUs (*repeated sensor units*), which are essentially the largest individual sensors that could fit within the design reticle, stitched together. A schematic illustration of the stitching process is shown in Figure 1.15. The diagram demonstrates how a reticle is divided into three parts: the left endcap, the RSU, and the right endcap. These RSUs are then stitched together to form a larger composite object. In the case of the MOSS, ten RSUs are stitched to create this stitched structure. Additionally, one left and one right endcap are attached to complete the assembly. The MOSS testing system is fairly large, especially when testing all ten RSUs. To address this, a smaller prototype called BabyMOSS was developed, consisting of just one RSU and the endcaps stitched to it, but retaining all the features of the RSUs in the full MOSS system. The RSU is

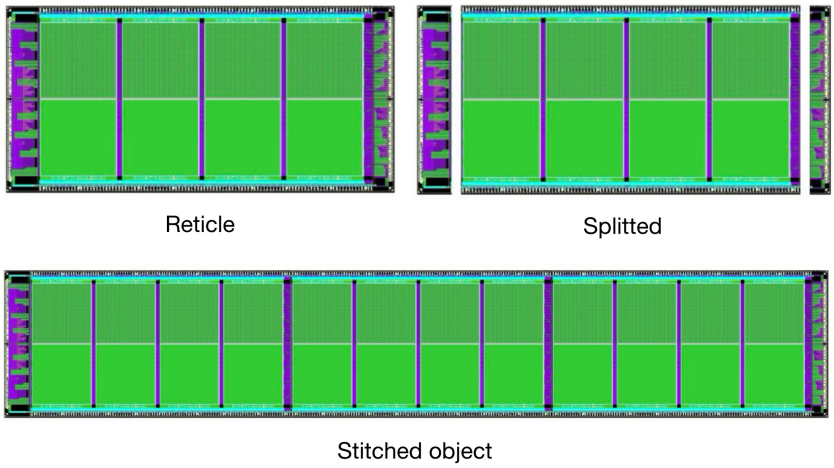


Figure 1.15.: Schematic of the stitching process (edited).[23]

made up of two half-units (HUs), which are called top and bottom, with each of them being composed of four matrices, also called regions. The regions of the top HUs have 256×256 pixels with a pixel of pitch 22.5 µm, while the matrices of the bottom HUs have 320×320 pixels with a pixel pitch of 18 µm.[24, 23]

Figure 1.16 illustrates the analogue in-pixel front-end circuitry, highlighting eight key settings that influence sensor operation. These settings are divided into four current controls—I_{RESET}, I_{db}, I_{bias}, and I_{biasn}—and four voltage controls—V_{casn}, V_{shift} (labeled as V_S in Figure 1.16), V_{casb}, and V_{psub}. Among these, V_{casb} is the most critical as it directly affects the threshold; an increase in V_{casb} lowers the threshold, which in turn raises the sensor's noise level.[25]

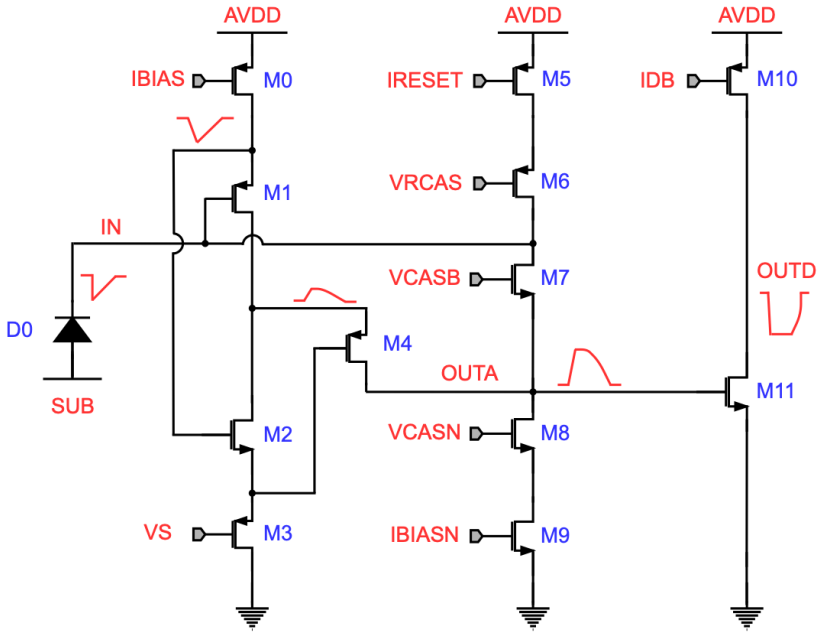


Figure 1.16.: Simplified schematic of the analog in-pixel front-end.[24]

V_{psub} determines whether the circuit is in a biasing or reverse biasing mode, with all other settings needing adjustment when reverse bias is applied. I_{RESET} governs the current flowing through the M7 diode, which influences the threshold, while V_{rcas} is linked to the I_{RESET} current mirror and is not adjustable. The current from diode D0 also passes through M7, so to maintain stable threshold levels, this leakage current must ideally be smaller than or equal to I_{RESET}.[25]

Each region has a different front-end variant, so that it can be examined, which region operates the best. The changes can be seen in Figure 1.4.

Table 1.4.: Different front-end variants within a half-unit.[24]

	Region 0	Region 1	Region 2	Region 3
TOP	Standard	Larger input transistor (M1)	Larger discriminator input transistor (M11)	Larger common-source transistor (M2)
BOTTOM	Standard	Standard	Standard	Reduced parasitic capacitance

2. Experimental Setup and Procedure

2.1. Setup

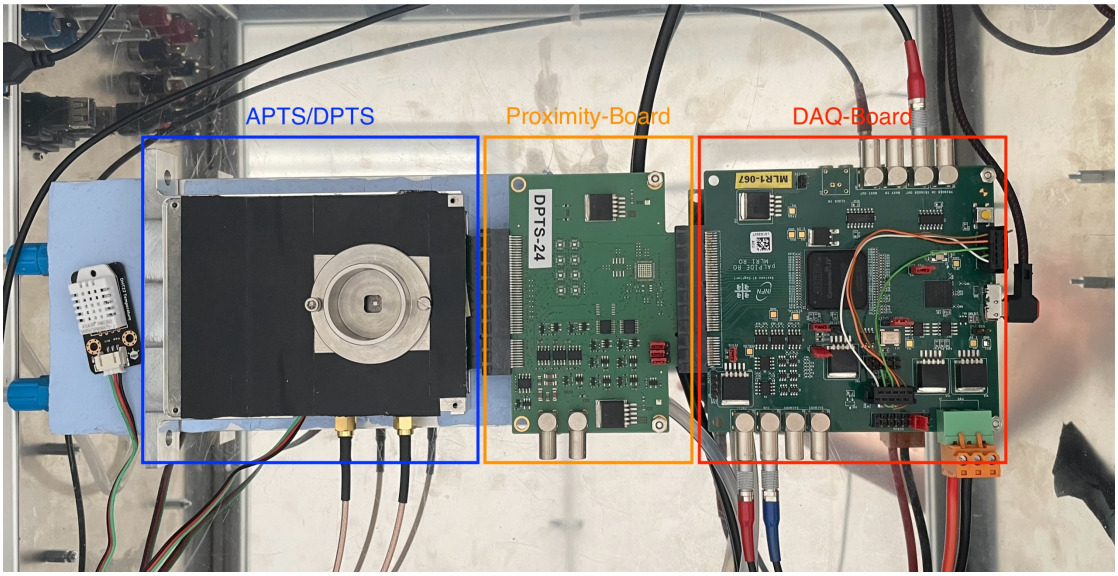


Figure 2.1.: Setup of the APTS/DPTS with the chip's closed housing, containing the APTS/DPTS and one of the DHT22 sensors, next to the Proximity-Board and the DAQ-Board (from left to right).

The setup of the APTS and DPTS are very similar and can be seen in Figure 2.1. On the left is the aluminium housing of the APTS/DPTS carrier card, which contains the fragile chip to protect it from impact and mechanical contact. With the help of nuts, bolts and plastic spacers, the chip is securely mounted, ensuring that it floats in the air and does not touch the aluminium casing. Additionally, the DPTS carrier card has to be connected to a PICOSCOPE 6424E via two SMC connectors. In Figure 2.1, these are the two similar-looking cables emerging from the bottom of the housing. Next to it, highlighted in orange in the picture, is the Proximity Board, which is specific to the type of chip being tested. Its purpose is to supply the necessary currents to the APTS/DPTS and make a connection between the chip and the DAQ Board. The DAQ (*Data Acquisition*) Board contains an FPGA and facilitates the readout and communication between the PC and the APTS via a USB cable that can be seen on the very right in the picture. Voltage from the power supply is delivered to the chip through the DAQ Board, which also supplies the back bias V_{BB} via two LEMO cables at the bottom, using negative polarity. The LEMO cable at the top is only needed for the DPTS setup and connects the TRIGGER OUT of the DAQ Board with the picoscope.

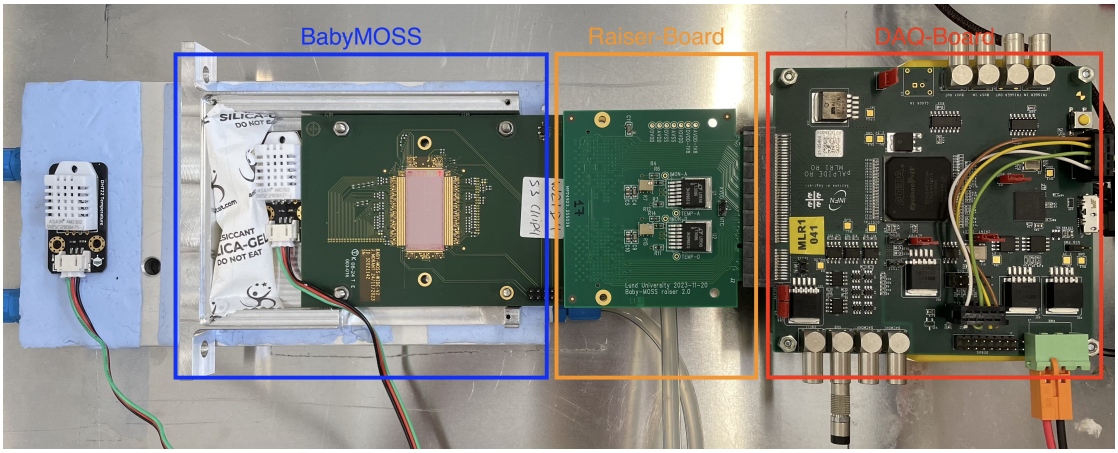


Figure 2.2.: Setup of the BabyMOSS with the chip's opened housing, containing the BabyMOSS and one of the DHT22 sensors, next to the Raiser-Board and the DAQ-Board (from left to right).

In order to make measurements with the BabyMOSS, the setup has to be changed. Instead of a Proximity Board, a Raiser Board is used as an interface between the BabyMOSS carrier card and the DAQ Board. The setup is shown in Figure 2.2

Following adjustments were made to make the setups suitable for temperature measurements. First, the entire setups were placed inside a large metal box to shield the setup from changes in the room temperature and create a more stable environment. A Huber Minichiller[26] was used to control the temperature of the setup by circulating tempered water through a aluminum plate beneath the chip's casing. A thermally conductive adhesive tape, visible in Figure 2.1 as the light blue surface under the DPTS box, was placed between the casing and the cold plate. To maximize thermal contact between the casing and the aluminum plate, the bolts securing the carrier card from the outside of the box were replaced with countersunk bolts, allowing the housing to lie flat on the plate. Since a temperature gradient can develop between the chiller and the detectors—because the coolant tubing is partially exposed to the room—an external temperature and humidity monitoring system was introduced. This was achieved using an Arduino Nano microcontroller and two DHT22 sensors, which are shown in Figure 2.2. They are able to capture data in the ranges -40–80°C and 0–100% relative humidity while having small uncertainties of ≤ 0.5°C and ± 2%[27]. One sensor is placed outside the housing but inside the large box, while the other is placed inside the carrier card box to measure the temperature and humidity as close to the chip as possible, ensuring precise data collection. Additionally, a LCD-panel was positioned outside the large box, allowing for live readout of the two sensors without opening the box and interfering with the measurement.

A schematic sketch of the whole APTS setup with the modifications for temperature measurements is shown in Figure 2.3.

After conducting several tests, it was determined that it takes approximately 2 hours to ensure the chip has fully thermalized. This conclusion is illustrated in Figure 2.4, where time in seconds is plotted on the x-axis and temperature in °C on the y-axis.

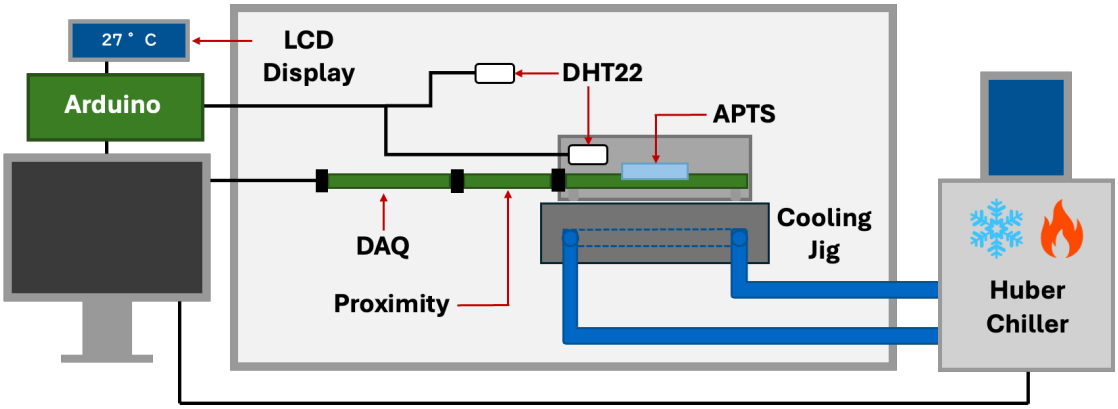


Figure 2.3.: Sketch of the APTS setup used.

In this case, the set point temperature at the Huber Minichiller was changed from 15°C to 30°C. As the temperature increases, the maximum amount of water vapor that the air can hold also rises, leading to a decrease in relative humidity. After 2 hours, the conditions stabilize, confirming that the chip has reached thermal equilibrium. Measurements were only taken after this point.

One risk that needed to be avoided was condensation forming on the chip. Most of the measurements were conducted in a temperature range from 5°C to 45°C, but with the ambient lab temperatures reaching 31°C and humidity levels up to 45%—resulting in a dew point as high as 17.7°C[28]—a way to lower the humidity had to be found. To address this, a thermally insulated jug was filled with liquid nitrogen and placed inside the closed large box, allowing the nitrogen to slowly evaporate. Since nitrogen gas is naturally dry and does not hold any moisture, it gradually fills up the box, replacing the moisture-laden air and thus reducing the humidity. Additionally, a package of silica gel was placed inside the housing due to its moisture-absorbing properties. In the event that any condensation forms, it will be absorbed immediately.

2.2. Measurement Methods

All the measurements described below were executed using an automatization script which ensures stable conditions in terms of measurement timing, duration and replicability.

2.2.1. Gain Scanning

One important characteristic of the APTS that was measured, is the gain. It is defined as the ratio of the baseline to V_{RESET}, so it's a measure of how much the voltage is amplified by the circuit. An exemplary gain calibration is shown in Figure 2.5. In the left panel, the baseline in mV is plotted as a function of V_{RESET} in mV, with each line representing a single pixel out of the 16. The right panel displays the numerically calculated derivative of the curves on the left, also as a function of V_{RESET}. It can be observed that the derivative remains relatively constant in the operating range of

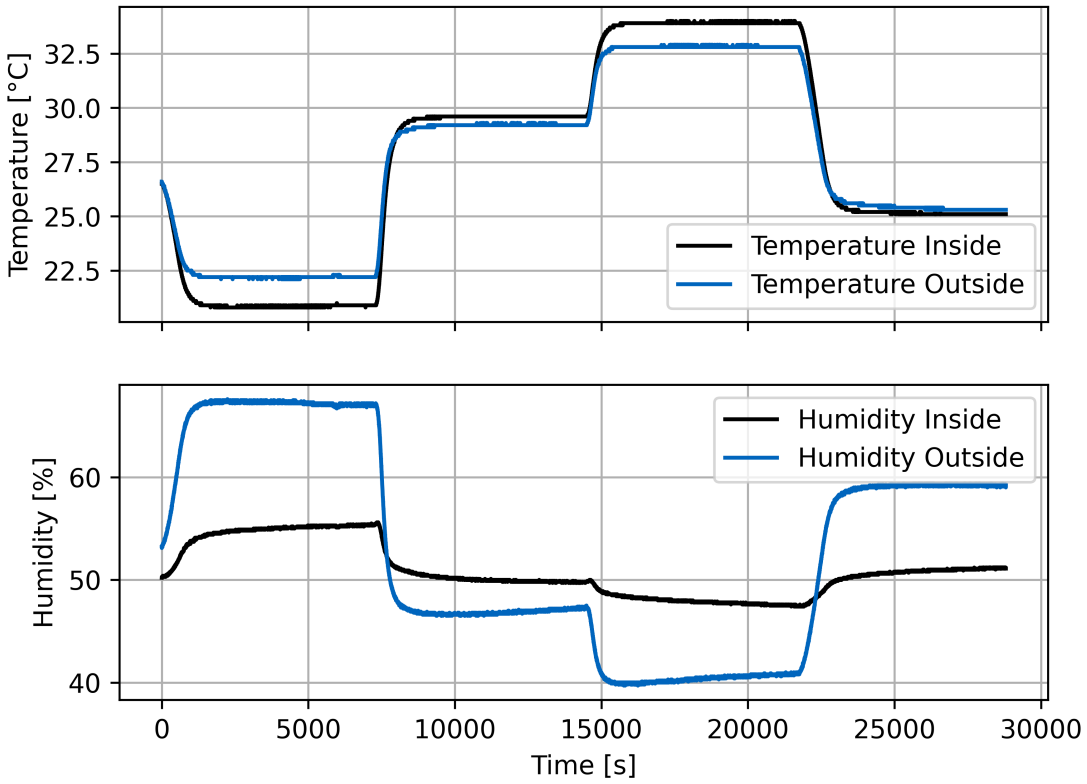


Figure 2.4.: Exemplary capture of the temperature and humidity with the DHT22 sensors for several temperature changes at the Huber chiller [20, 30, 35, 25]°C.

V_{RESET}, particularly around the standard value of 500 mV. The linearity establishes a consistent calibration factor linking signal voltage to ADC counts. Maintaining this linearity is crucial for accurate energy calibration, as deviations can cause issues.

The measurement was done by changing the V_{RESET} in steps of 10 mV in the range of 20–900 mV, and looking at the readout from the baseline. This was done for the 10^{14} MeV n_{eq} cm^{-2} and the 10^{15} MeV n_{eq} cm^{-2} irradiated chip in the temperature range 5–30°C in steps of 2.5°C.

As shown in Figure 2.5, the graphs are not continuous. Initially, the baseline does not change with variations of V_{RESET}, but after a certain threshold is reached, it begins to rise linearly following an immediate offset. The points where the graphs are discontinuous are referred to as "jump points" and the discontinuities themselves are called "gain jumps". Before the gain abruptly increases at the jump points, the pixels are "dead" meaning when pulsing them (see subsection 2.2.2), no hit will be triggered, and thus, the waveform will just consist of noise.

2.2.2. Waveform Analysis

For the APTS and the DPTS, waveforms were read out and analyzed. The pixels were pulsed, and their output signals were recorded with the picoscope. Different techniques

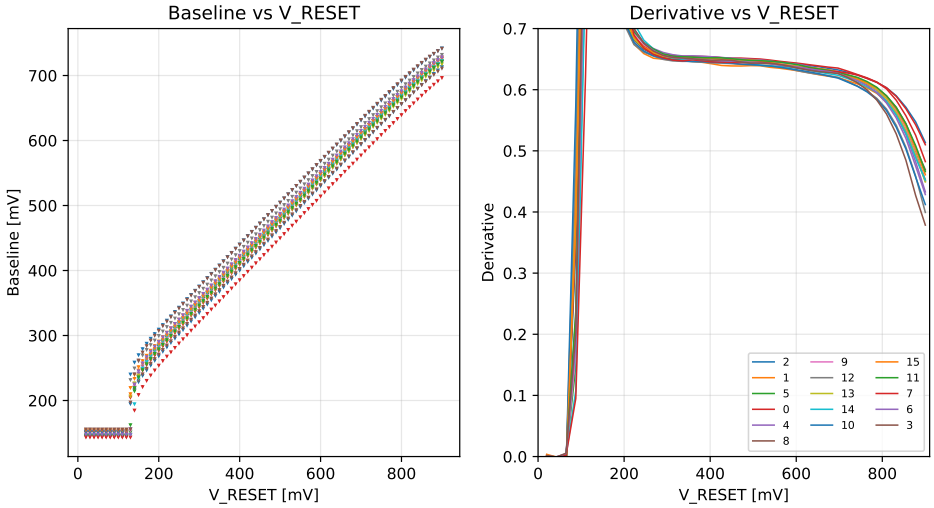


Figure 2.5.: Exemplary gain scanning of the Irr14 sensor with a back bias of $V_{BB} = 1.2\,V$ at $T = 20°C$.

were used to pulse the pixels for each type of chip.

To pulse the APTS, a Breakout Board was used, positioned between the Proximity Board and the APTS carrier card. This modification of the setup allowed the direct injection of signals to the sensor without relying on the DAQ Board, which is important since it was observed in previous studies[29] that the DAQ Board can introduce interference on the analog signal lines. Then, with the arbitrary waveform generator (AWG), a rectangular waveform of 1 kHz with an amplitude of $\sim 1.2\,V$ was fed back into channel B of the picoscope, as well as into the pulsing input TRG, labeled $\text{TRIGGER}_{\text{inj}}$ in Figure 1.11. This emulated the shape of the internal trigger pulse and enabled the pulse. The analog output of one pixel was then read out via the Breakout Board, in this work, pin 38 was selected on the Breakout Board, corresponding to one of the central pixels as shown in Figure 2.6. The signal was then captured by channel A of the picoscope and recorded. The schematic of the modification can be seen in Figure 2.7. The height of the pulse is determined by V_H, which was set to values between 0.2 V and 1.2 V in steps of 0.2 V. Measurements were conducted for all three APTS chips, with the back bias set to $V_{BB} = [0.0, 1.2, 2.4, 4.8]\,V$ in the standard temperature range. For each setting, 1000 waveforms were recorded and saved.

An exemplary waveform of the APTS AF15P_W22B11 can be seen in Figure 2.8. The time in ns is situated on the x-axis, while the measured output voltage in mV is on the y-axis. This waveform was captured with a back bias of $V_{BB} = 2.4\,V$ and a pulse height of 1.0 V.

To obtain the baseline, the average of all captured points at $t < 0$ was calculated to minimize noise influence. The amplitude was then determined by finding the difference between the baseline and the waveform's minimum. To calculate the slope of the falling edge, a linear function was fitted to the data. The fitting range was dynamically adjusted for each waveform based on its amplitude, setting the upper

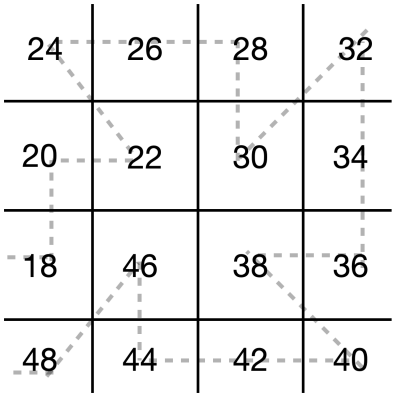


Figure 2.6.: Mapping of the APTS pixels. The numbers correspond to the pins on the Breakout Board.

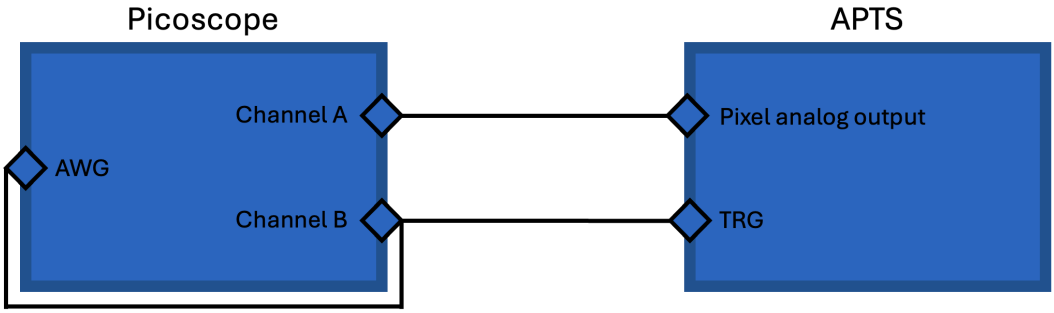


Figure 2.7.: Schematic of the APTS pulsing.

bound at 5% below the baseline and the lower bound at 50% below it. The slope was derived from this linear fit. The reason for this dynamic range is the additional peak observed at the falling edge in Figure 2.8, which had to be excluded from the fitting range to avoid skewing the fit. This extra peak likely results from capacitive coupling with the current-carrying wires of the DHT22 sensors or from signal reflections, and could not be avoided during waveform capture. These steps were repeated for all 1000 recorded waveforms, and the mean values of the obtained values were taken to smooth out statistical fluctuations caused by noise like capacitive coupling.

For the pulsing of the DPTS, a different method was used. In this case, only one pixel—specifically (15,15)—was pulsed using the DAQ Board with a V_H of 0.6 V for the standard temperature range. The output signals from the pixel were read out through the SMA outputs on the carrier card, which were connected to the picoscope. For every setting, 500 waveforms were recorded and saved for the analysis.

An exemplary waveform of the used DPTS "O" is shown in Figure 2.9. Here, the time in ns is on the x-axis, and the two outputs recorded by the picoscope, OUT_P and OUT_N in mV, are on the y-axis.

To calculate the signal amplitude, the maximum of OUT_N was subtracted by OUT_P, and the result was divided by 2. This is illustrated by the grey "Pulse Height" line in

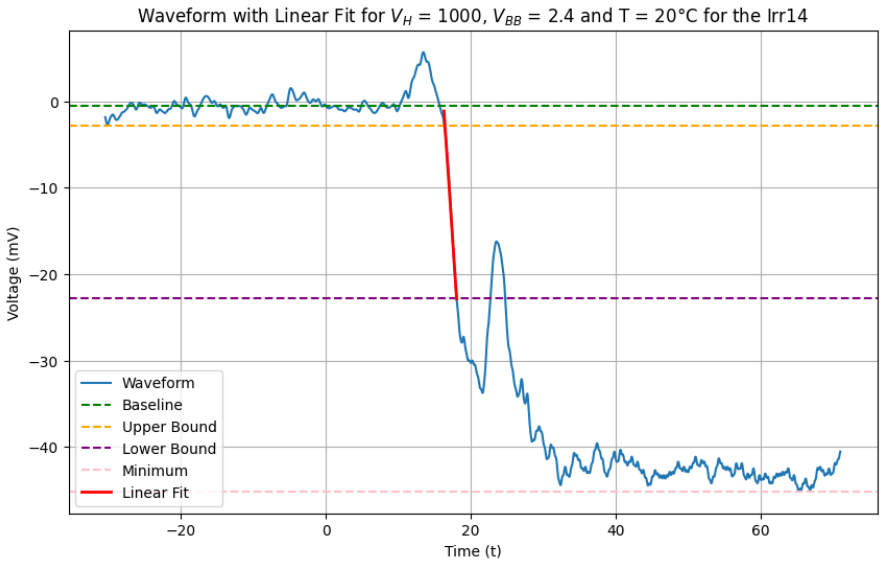


Figure 2.8.: Exemplary waveform of the analog signal falling edge from the APTS.

Figure 2.9. The midpoint of the two waveforms, where they intersect, was determined by summing OUT_N and OUT_P and dividing by 2, shown as the light green horizontal line. Next, the slope of the first rising edge was calculated by fitting a linear function to it. To set the fitting range dynamically, the crossing points had to be interpolated because the picoscope reached its time resolution limits. Around this crossing point, a window of 5 captured entries was defined, which was used as the fitting range. A exemplary result of the fitting range in the Figure 2.9 can be seen in orange.

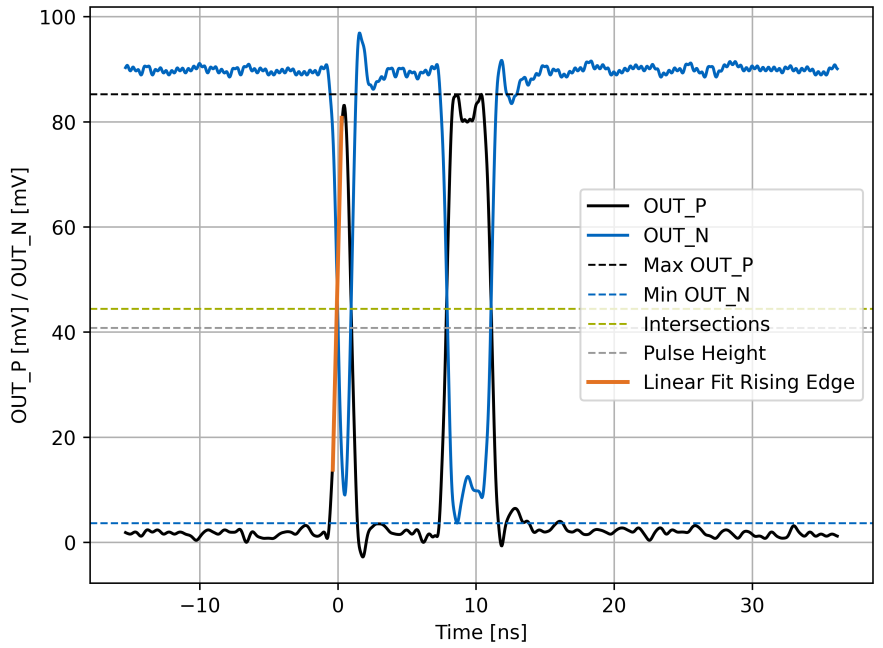
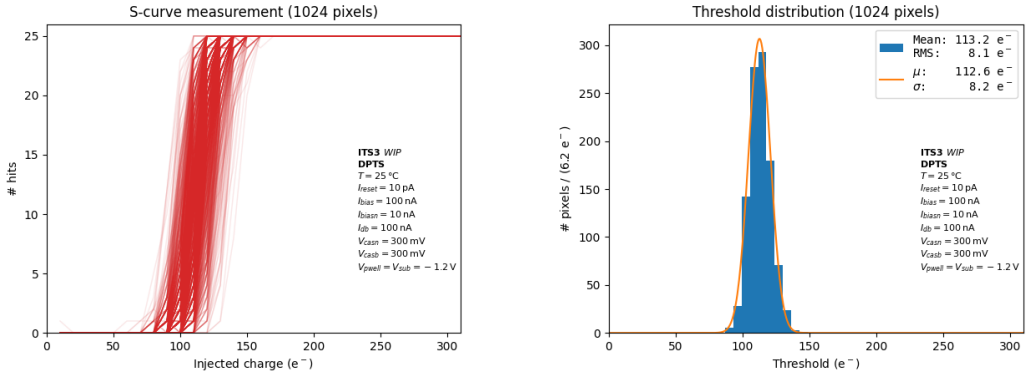


Figure 2.9.: Exemplary waveform of the digital time encoded output of the DPTS.

2.2.3. Threshold and Noise

To register a hit after a pixel is pulsed, both the DPTS and BabyMOSS use a pixel-specific threshold. If the charge deposited or injected into the pixel is below this threshold, no signal is detected. However, if the charge exceeds the threshold, a hit is recorded. Since the threshold is influenced by different parameters like V_{CASB} or temperature, it is crucial to know the chips threshold for a maximized detection efficiency. This can be done by injecting a range of test charges via the pulsing capacitance C_{inj} and measuring how many hits are registered. An example can be seen in Figure 2.10a. Here, a DPTS was pulsed 25 times for each step, ranging from $10\,e^-$ to $310\,e^-$ in increments of $10\,e^-$. The resulting plots are referred to as s-curves due to their characteristic S-like shape. The point at which a pixel detects 50 % of the pulses is defined as its threshold. To determine the noise, a Gaussian fit is applied, which is the derivative of the s-curve, with the mean representing the threshold and the standard deviation corresponding to the pixel's noise level. Since these steps are repeated for all the pixels, a threshold distribution is generated, as shown in Figure 2.10b. From this, the overall threshold of the entire chip is determined by fitting a Gaussian to the distribution. The procedure for the BabyMOSS is essentially the same, with the distinction that a separate threshold is calculated for each of the eight pixel matrices, rather than a single threshold for the entire chip.



(a) S-curve

(b) Threshold distribution

Figure 2.10.: Threshold of the DPTSOW22B54 at 25°C.

Additionally, one can define noisy pixels, meaning pixels that fire more often than they are expected to. This is done by introducing a frequency threshold, which is defined as $\frac{N_{hits}}{N_{trg}}$. Every pixel, that lies above an assigned frequency threshold, is considered to be noisy.

2.2.4. Fake Hit Rate

The fake-hit rate (FHR) refers to the number of hits detected by a single pixel in the absence of any pulsing or external stimuli. To measure this, a series of trigger pulses is sent from the DAQ Board to the oscilloscope without activating any pixels in the matrix. This is done by issuing a command to pulse the matrix but ensuring no pixels are

selected via the shift register. The FHR, also known as noise occupancy, is calculated using the formula:

$$FHR = \frac{N_{hits}}{n_{pixel} \cdot \Delta t_{WF} \cdot N_{trg}} \tag{2.1}$$

where N_{hits} is the total number of hits detected in the waveform, n_{pixel} the total amount of pixels in the matrix, Δt_{WF} the duration of the recorded waveforms and N_{trg} the number of trigger pulses sent, equivalent to the number of recorded waveforms.[30]

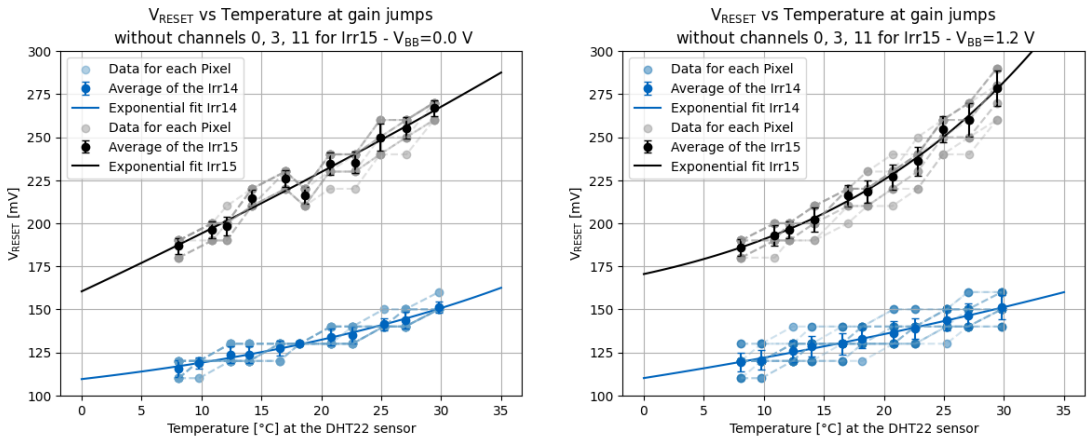
3. Results

3.1. APTS

This section presents the results obtained from the APTS.

3.1.1. Operating Range

Since it was observed that the jump points shift with temperature, this behavior was further investigated. The V_{RESET} values at the jump points were plotted as a function of the temperature measured by the DHT22 sensor near the chip for back biases of 0.0 V and 1.2 V, as shown in Figure 3.1. For both back bias values, V_{RESET} was found to increase with temperature and irradiation level. The mean V_{RESET} from 16 recorded pixels was taken at each temperature, with the standard deviation used as the error. An exponential function was then fitted to the averages. Due to malfunctioning pixels (channels 0, 3, 11) on the chip irradiated to 10^{15} MeV n_{eq} cm^{-2} at temperatures above 25°C, these were excluded from both the mean and the fit.



(a) $V_{BB} = 0.0\,V$ (b) $V_{BB} = 1.2\,V$

Figure 3.1.: Jump points as a function of temperature. Without channels 0, 3, 11 for the 10^{15} MeV n_{eq} cm^{-2} irradiated sensor.

One possible explanation for this phenomenon is the leakage current in the circuit. Leakage current in semiconductors depends on both irradiation levels and temperature, so it is expected that a more irradiated or warmer sensor will experience higher leakage current[12]. If this current becomes too large for V_{RESET} to compensate, the signal will fail to be amplified by the rest of the circuit. As a result, the baseline won't rise, and during pulsing, only noise will be captured. The jump points mark the threshold

where V_{RESET} becomes sufficient to overcome the leakage current. This behavior is particularly relevant when examining Figure 3.2, which shows the jump points of all pixels, including channels 0, 3, and 11, for the 10^{15} MeV n_{eq} cm^{-2}irradiated chip, plotted against temperature. A horizontal line at $V_{RESET} = 500$ mV represents the chip's standard operating value. As shown, at 27.5°C, two channels, and at 30°C, three pixels exceed this value, meaning they would appear dead during measurements. To recover functionality, a higher V_{RESET}, surpassing the jump points, could be applied. However, this may compromise the gain stability, as discussed in section 2.2.1.

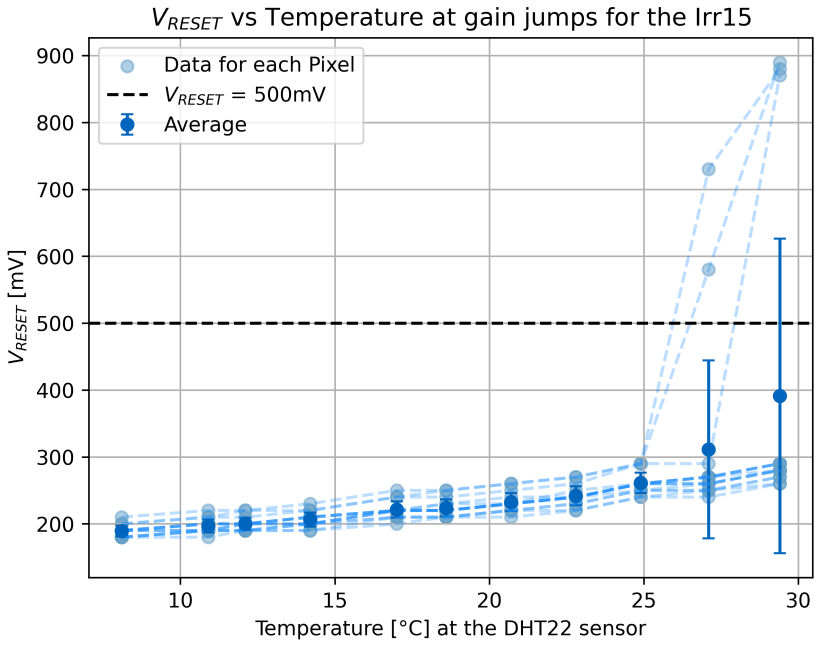


Figure 3.2.: Jump points of all channels as a function of temperature for the 10^{15} MeV n_{eq} cm^{-2} irradiated sensor.

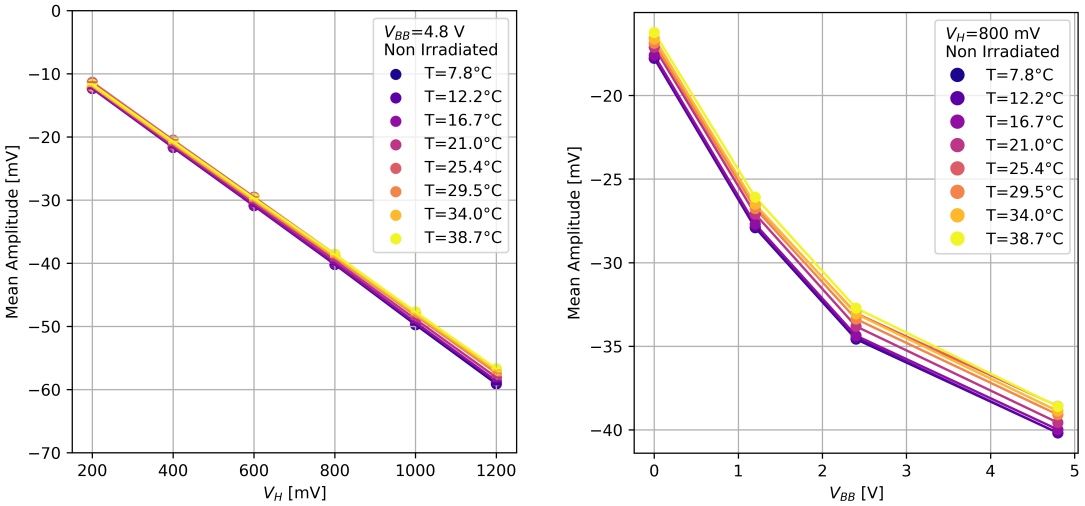
3.1.2. Pulse Analysis

After pulsing the three APTS, the following results were obtained.

First, the mean amplitude was plotted as a function of V_H for different temperatures in Figure 3.3a for the non-irradiated sensor with the back bias fixed at $V_{BB} = 4.8$ V. As expected, increasing the pulse height V_H led to a linear rise in the measured amplitude. With increased temperature, the absolute of the amplitude decreased slightly, with the effect becoming more pronounced at higher V_H.

In Figure 3.3b, a constant V_H of 800 mV was used to plot the mean amplitude as a function of back bias for the non-irradiated APTS. While increasing back bias raised the absolute of the signal, the relation was not linear like the response to V_H. Additionally, varying V_{BB} did not alter the temperature hierarchy.

When examining the effects of higher irradiation, the plots in Figure 3.4 provide key insights. In Figure 3.4a, the mean amplitude of the signal is shown as a function of V_H for the 10^{14} MeV n_{eq} cm^{-2} irradiated sensor, while Figure 3.4b presents the same for

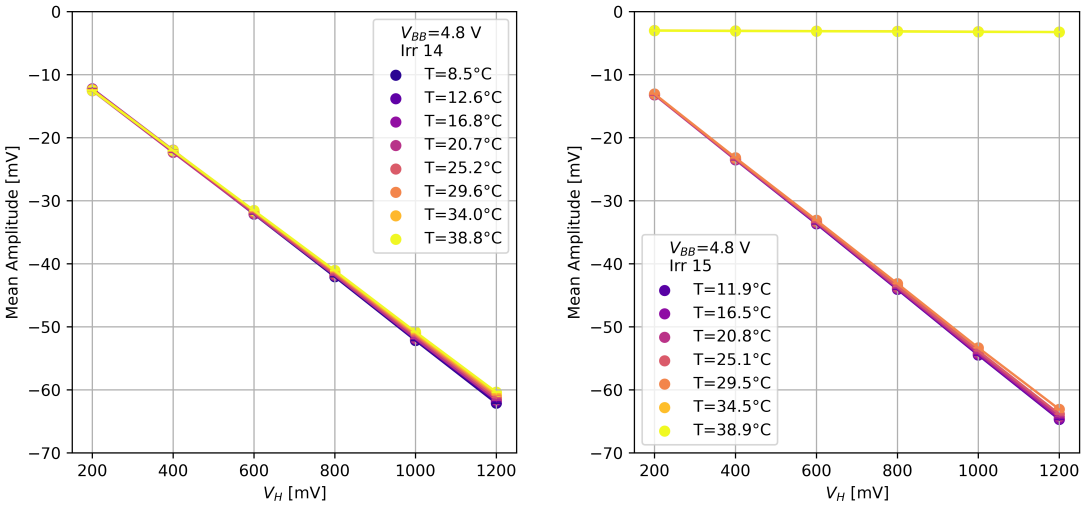


(a) Amplitude as a function of V_H.

(b) Amplitude as a function of V_{BB}.

Figure 3.3.: Measured amplitudes after pulsing the APTS.

the 10^{15} MeV n_{eq} cm^{-2} irradiated sensor. It can be observed that the 10^{14} MeV n_{eq} cm^{-2} irradiated APTS behaves similarly to the non-irradiated chip, at least within the examined range. In contrast, the pixel monitored on the 10^{15} MeV n_{eq} cm^{-2} irradiated chip stopped functioning at temperatures above 30°C, as evidenced by the two flat lines in the corresponding plot.



(a) Amplitude as a function of V_H for the Irr14 sensor.

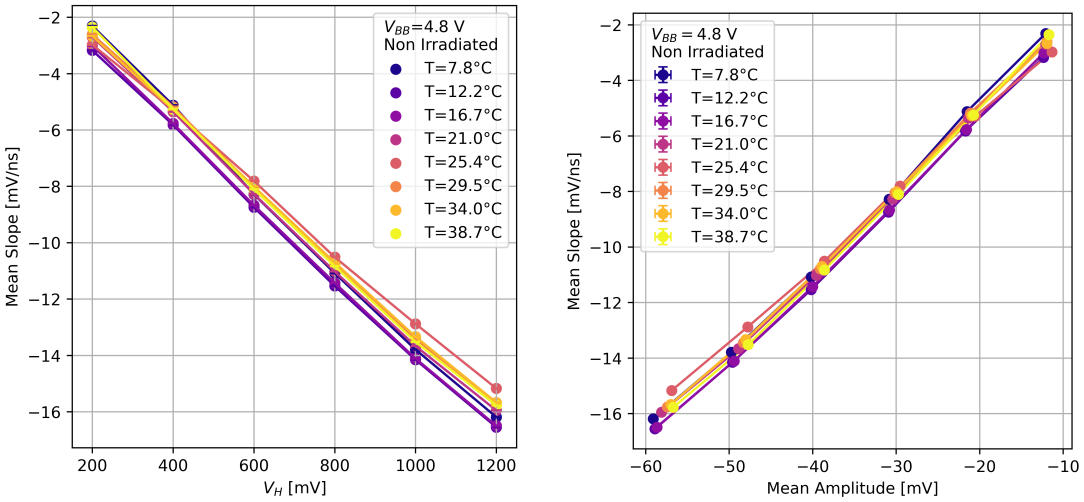
(b) Amplitude as a function of V_H for the Irr15 sensor.

Figure 3.4.: Measured amplitudes after pulsing the irradiated APTS.

When examining the temperature dependence of the falling edge slope, no clear trend was identified, as depicted in Figure 3.5. In Figure 3.5a, the slope is shown as a function of V_H. While higher temperatures generally result in a slightly lower

absolute of the slope, there are several outliers that deviate from this pattern. To further investigate, Figure 3.5b plots the slope on the y-axis against the amplitude on the x-axis to assess the linear relationship between V_H, amplitude, and slope. However, no consistent temperature-related trend is apparent.

Additional plots that support the general claims made from the exemplary settings presented here for the three chips can be found in the Appendix A.



(a) Slope as a function of V_H.

(b) Slope as a function of the Amplitude.

Figure 3.5.: Measured slopes after pulsing the APTS.

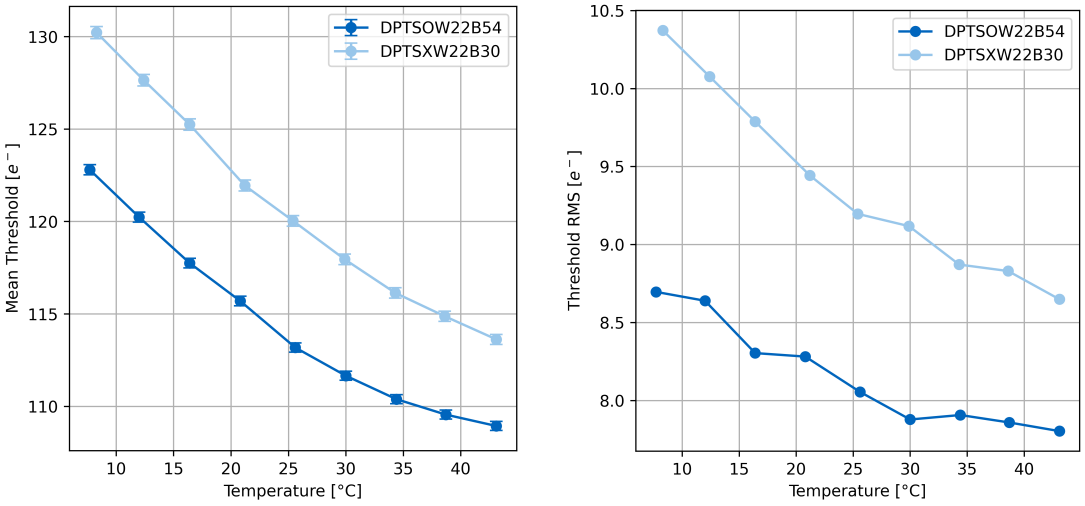
In summary, temperature has a minimal impact on the analog waveforms of the APTS. This behavior may be attributed to the fact that only the analog circuitry of the APTS is being pulsed, and this circuitry shows limited temperature dependence when in a non-irradiated state.

3.2. DPTS

In the following section, the results of the two examined DPTS will be presented and discussed.

3.2.1. Threshold and Noise

It could be observed, that the threshold of the DPTS chips is dependent on temperature, as shown in Figure 3.6a. Here, the mean threshold in units of elementary charges is plotted against the temperature at the two different chips and the error bars correspond to the RMS. It can be seen that the threshold decreases with increasing temperature, though not in a strictly linear fashion. According to the main DPTS paper [17], the threshold is expected to decrease by approximately $0.5\,e^-$ per degree Celsius within the $15-40$°C range. To verify this, a linear fit was applied to the data points in this range, yielding a slope of $(-0.37 \pm 0.03)\,e^-$ for the DPTS-O and $(-0.46 \pm 0.03)\,e^-$ for the



(a) Threshold (b) RMS

Figure 3.6.: The threshold and the RMS as functions of temperature.

DPTS-X. These values, particularly for the base version chip, deviate from the expected result reported in the paper.

Another aspect investigated was how the RMS, representing the size of the error bars, scales with temperature. Figure 3.6b shows the RMS of the threshold in e^- as a function of temperature. It is evident that the RMS decreases as temperature rises, indicating that the thresholds across all pixels have less variance and converge toward a more uniform value at higher temperatures. Consequently, the s-curves become narrower.

Another parameter that was investigated is the noise of the pixels. This relation is shown in Figure 3.7, where the mean noise in elementary charges is plotted as a function of temperature for both chips. It can be seen, that the noise increases, meaning the rising edge of the s-curves are less steep.

One explanation for this behavior is that the threshold decreases as certain properties of the CMOS transistors are influenced by temperature changes, resulting in variations in the current, which in turn affect the threshold. Additionally, the increase in thermal noise contributes to this effect by raising the baseline, bringing it closer to the threshold. As a result, a smaller signal is needed to cross the threshold and register a hit, effectively lowering the overall threshold.

3.2.2. Fake Hit Rate

The fake hit rate of the examined DPTS detectors is displayed in Figure 3.8. Here, the temperature at the sensor is on the x-axis and the fake hit rate in $s^{-1}pixel^{-1}$ on the y-axis. For visibility reasons, the voltage V_{casb} was increased to 350 mV instead of the standard 300 mV, to lower the threshold and thus increase the fake hit rate of the chips. For both detectors, an increase in the fake hit rate can be observed. The reason for this is that, since the threshold decreases for higher temperatures, a smaller fake hit is needed to trigger the pixels, increasing the probability of having fake hits.

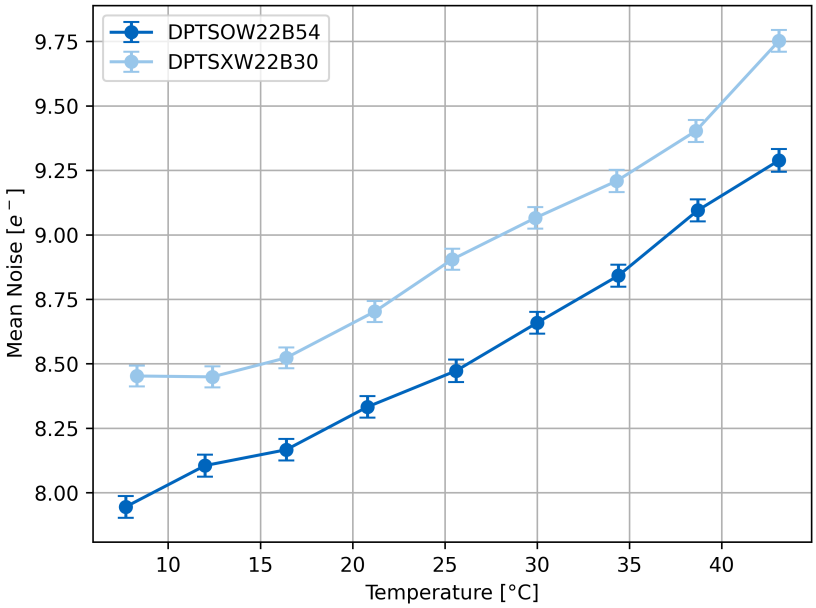


Figure 3.7.: Mean Noise of the DPTS as a function of temperature.

3.2.3. Timing Parameter

Next, influence of temperature of the parameters used for the encoding are analyzed. For a better comparison, they were normalized with the design simulation values provided in Table 1.3. To obtain these values, a decoding scan was performed, producing a data frame where each pixel was assigned a T_{PID} and a T_{GID} value. These values

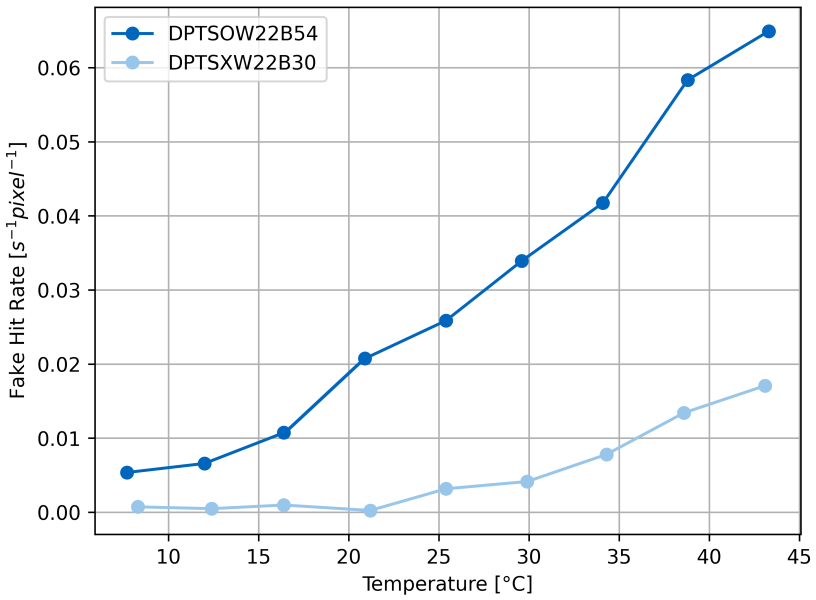
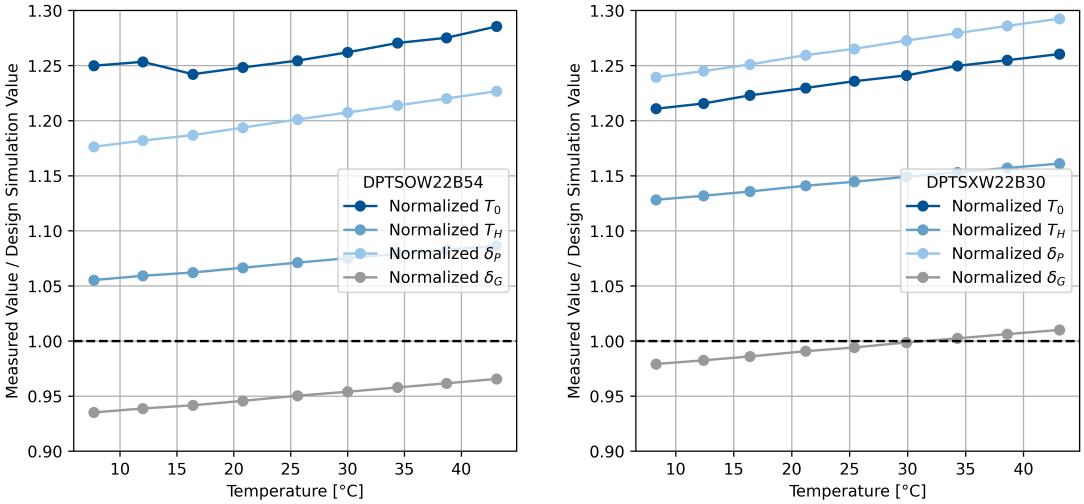


Figure 3.8.: Fake Hit Rate of the DPTS as a function of temperature.



(a) DPTSOW22B54 (b) DPTSXW22B30

Figure 3.9.: Normalized timing parameters of the two DPTS examined as a function of temperature.

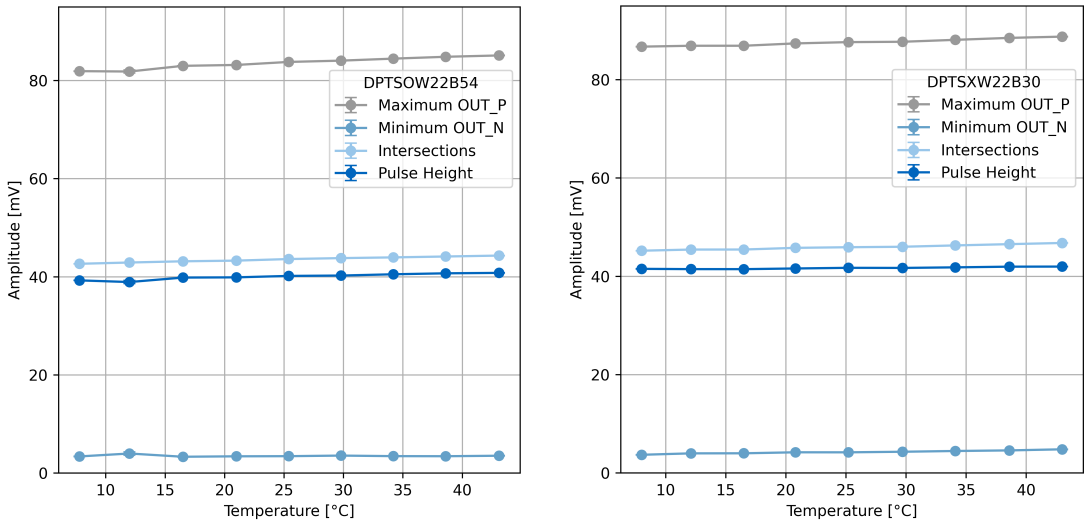
were then fitted to equations 1.1 and 1.2, respectively, yielding a T_H and δ_P for each row and a T_0 and δ_G for each column. These parameters were subsequently averaged to provide the final values. Additionally, the chequered pattern of the DPTS-X was not decoded to replicate the results of Cecconi et al[19] that were working with the same chip. The results can be seen in Figure 3.9, where the measured values of the timing parameters is divided by the design simulation values as a function of temperature for both chips. It can be seen that T_0, T_H and δ_P are above the expected value, while δ_G is below it, except for the DPTS-X for temperatures above 30°C.

This observed increase of the timing parameters is expected according to Formula 1.4, since the delay is proportional to $T^{\frac{3}{2}}$. Also, when comparing the yielded results from Figure 3.9b with the results from Cecconi et al[19], one can determine the ambient lab temperature to be between 15°C and 20°C.

3.2.4. Pulse Analysis

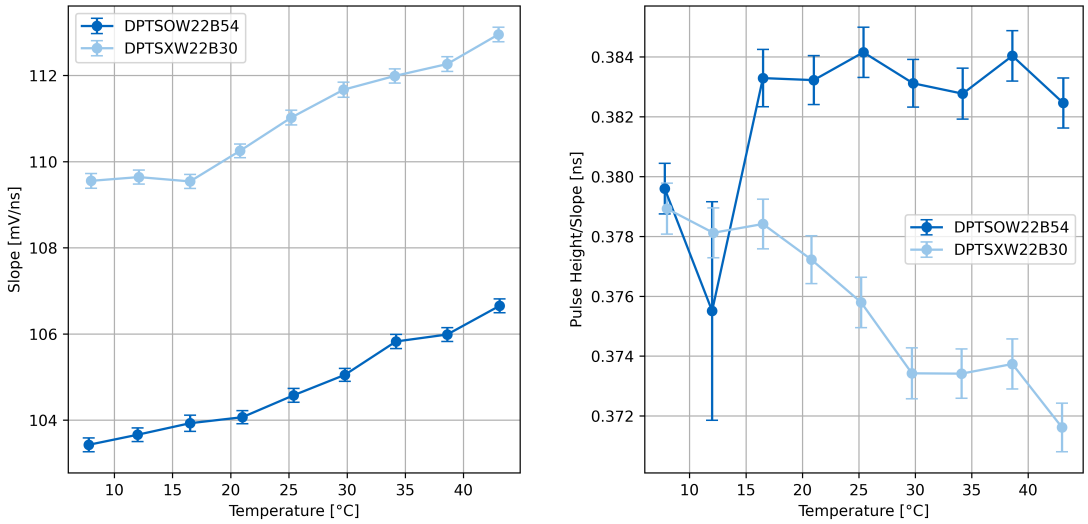
The results of the pulsing are shown in Figure 3.10, where the mean amplitudes of various parameters of the two DPTS chips are plotted on the y-axis, and the temperature is displayed on the x-axis. While the effect of temperature is minimal, it is noticeable that the amplitude increases slightly as the temperature rises.

The impact of temperature on the slope of the first rising edge is illustrated in Figure 3.11a, where the slope, measured in $\frac{\text{mV}}{\text{ns}}$, is plotted as a function of temperature. For both chip variants, the slope increases with rising temperature, which would typically result in a faster rise time and, consequently, improved timing performance. However, since the pulse height also scales with temperature, potentially counteracting this improvement, a more detailed analysis is presented in Figure 3.11b. By dividing the pulse height by the slope, the dominant effect was examined. The results show that the



(a) DPTSOW22B54 (b) DPTSXW22B30

Figure 3.10.: Measured amplitude of the DPTS pulsing as a function of temperature.



(a) The slope of the first rising edge of the DPTS as a function of temperature.

(b) The slope of the first rising edge of the DPTS divided by the pulse height.

Figure 3.11.: Results of the DPTS pulsing.

rise time of the DPTS-X decreases as temperature increases, whereas for the DPTS-O, the rise time remains relatively stable above 15°C.

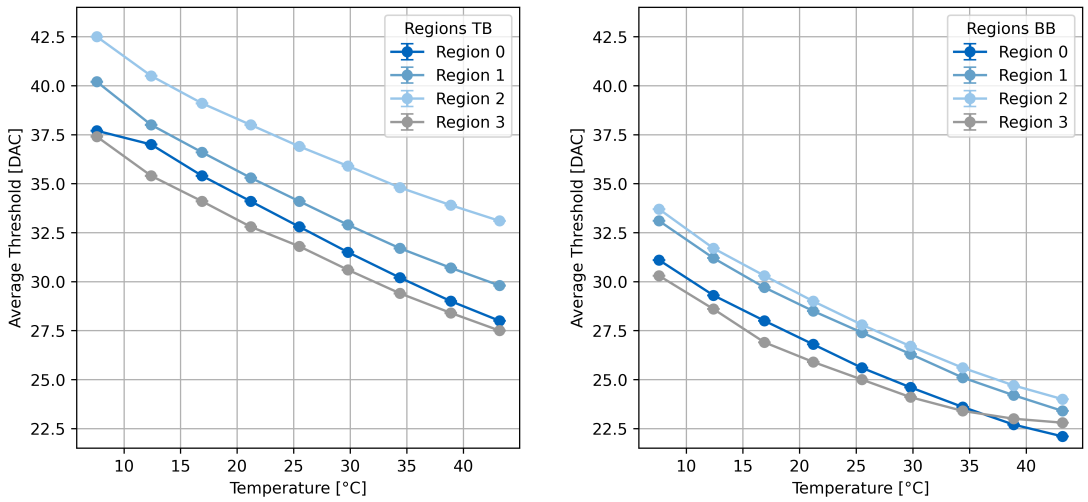
3.3. BabyMOSS

In the following section, the results of the BabyMOSS are presented. Since no energy calibration has been done yet, the measurements are measured in DAC units instead of

e^-. The BabyMOSS contains eight distinctive regions, thus the data visualization was arranged by the two half-units to provide clearer insight and better readability.

3.3.1. Threshold and Noise

First, the effect of temperature on the threshold was analyzed, as illustrated in Figure 3.12. The average threshold in DAC units is plotted against temperature for the different regions. As with the DPTS, it is evident that the threshold decreases as the temperature rises.



(a) Top HU

(b) Bottom HU

Figure 3.12.: The average threshold of the pixels in each region as a function of temperature.

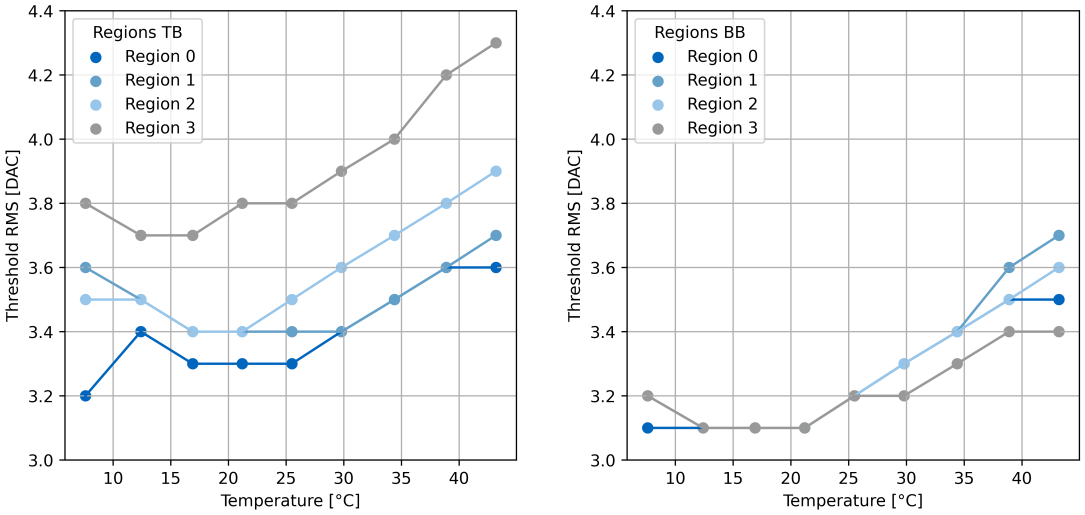
One parameter that behaves differently compared to the DPTS is the RMS of the threshold. In Figure 3.13, the RMS, which represents the size of the threshold's error bars for the BabyMOSS, is plotted as a function of temperature in DAC units for the two HUs. Unlike the DPTS, where the RMS decreases with rising temperature, here it actually increases as the temperature goes up.

Similar to the DPTS, the noise of the pixels increases for all regions with increasing temperatures, as can be seen in Figure 3.14. Here, the noise, so the standard deviation of the derivative of the s-curve, is plotted as a function of temperature.

Next, the influence of temperature on the amount of noisy pixels is examined. For the plots in this section, a noisy pixel is defined with a frequency threshold of 0.01. In Figure 3.15 it is shown, that the amount of noisy pixels scales with temperature.

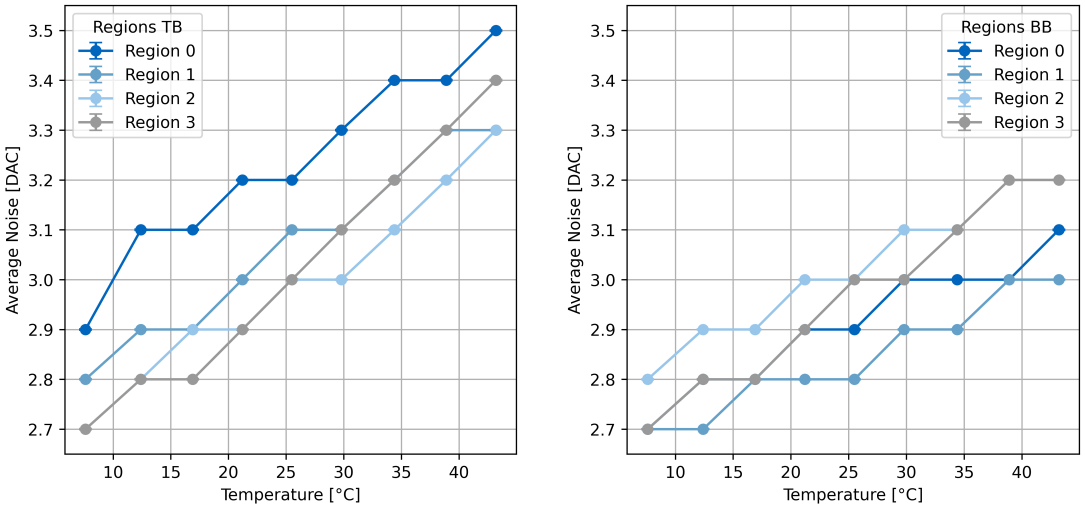
3.3.2. Fake Hit Rate

One important parameter that was examined is the Fake Hit Rate. To improve the quality of the plots, a mask had to be obtained. For this, the frequency threshold was set to a lower value of just 0.001 $\frac{\text{hits}}{\text{trigger}}$ and the noisy pixels above this threshold were masked. Since the amount of noisy pixels increases with an increase in temperature like



(a) Top HU (b) Bottom HU

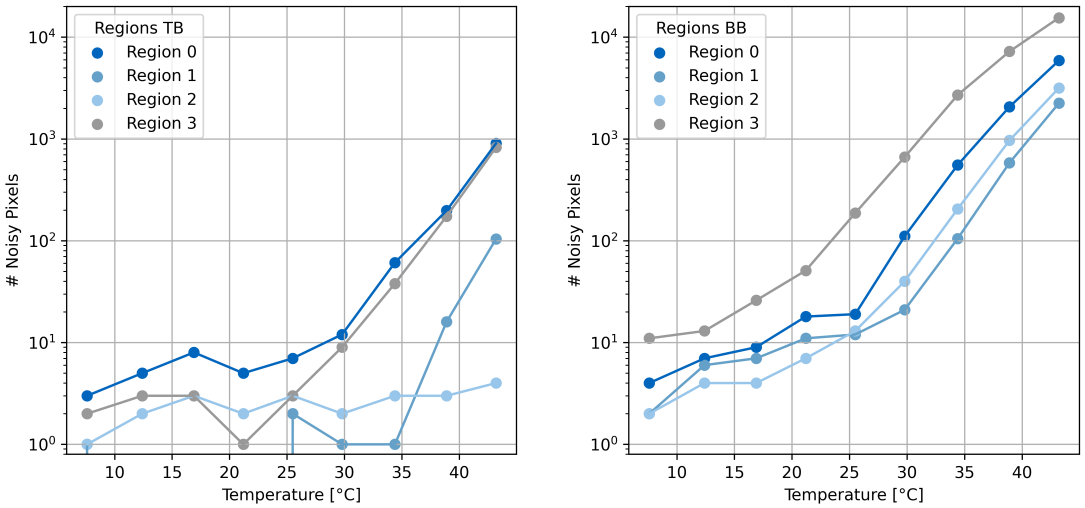
Figure 3.13.: The average RMS of the threshold the pixels in each region as a function of temperature.



(a) Top HU (b) Bottom HU

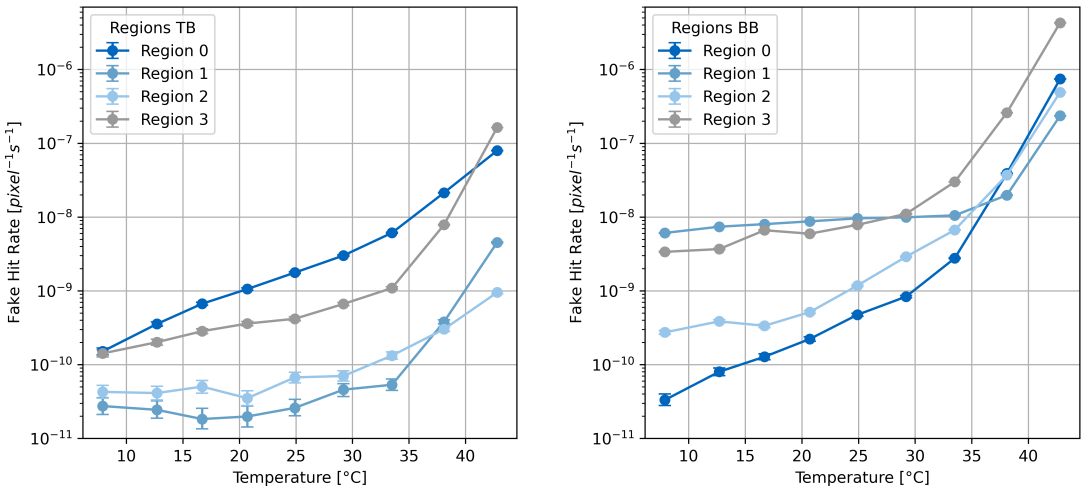
Figure 3.14.: The average noise of the pixels in each region as a function of temperature.

mentioned before, the mask of the 45°C measurement was taken for all the temperatures. The results are presented in Figure 3.16. In this, the Fake Hit Rate in pixel^{-1}s^{-1} is plotted as a function of temperature for all the regions. Above temperatures of 35°C, the incline increases for all regions compared to temperatures below that. While the FHR reaches the order of 10^{-6} pixel^{-1}s^{-1} for a temperature of 45°C, it stays below 10^{-7} pixel^{-1}s^{-1} for all regions and temperatures under 35°C.



(a) Top HU (b) Bottom HU

Figure 3.15.: Number of noisy pixels as a function of temperature as a semi-logarithmic plot.



(a) Top HU (b) Bottom HU

Figure 3.16.: Fake Hit Rate as a function of temperature as a semi-logarithmic plot.

4. Summary and Outlook

During the upcoming upgrade of the Inner Tracking System, the Inner Barrel of the ITS2 will be replaced by three bent, wafer-scale, silicon-only cylindrical layers. Each of these layers will consist of two stitched half-barrels to significantly reduce the material budget. In addition, a shift from water-cooling to a gas-cooled system will further lower the material budget.

To ensure that the upgraded system fulfills its physics objectives, extensive testing of these new technologies is essential. Several test structures have been developed for this purpose. This work examines the influence of temperature on three different test structures: the Analogue Pixel Test Structure (APTS), the Digital Pixel Test Structure (DPTS), and the BabyMOSS.

In order to test the temperature influences on the performance of the prototype sensors, a new setup was constructed as follows. The chips with the entire data acquisition modules were housed inside a metal box to shield it from external temperature fluctuations, ensuring stable and accurate measurements. A Huber Minichiller circulated temperature-controlled water through an aluminum plate beneath the chip casing, with countersunk bolts and thermally conductive tape used to maximize thermal contact. An Arduino-based monitoring system equipped with DHT22 sensors tracked temperature and humidity both inside and outside the housing. The system required approximately 2 hours to reach thermal equilibrium before measurements could begin. To prevent condensation, liquid nitrogen was employed to reduce humidity by replacing the moisture-laden air within the box.

The operating range of the APTS was first investigated by analyzing gain discontinuities in irradiated chips. It was found that as temperatures and irradiation levels increase, a higher V_{RESET} is required to overcome leakage current and restore pixel functionality. For the 10^{15} MeV n_{eq} cm^{-2} irradiated chip, pixel degradation became apparent at temperatures exceeding 25°C, causing some pixels to become dysfunctional under standard operational settings. Additionally, a pixel from each of the three APTS was pulsed, with the resulting analog waveforms captured and studied. It was found that a change in temperature influences the analogue pulse shape only minimally as long as it is within its operating range, especially compared to a change in other parameters like the pulse height or the back bias. For the future, detector designers should thus focus on precise temperature control and anticipate the need for adjustments in the operational settings to ensure pixel functionality under irradiation.

The first parameters studied for the DPTS were the threshold and noise. It was observed that the threshold decreases, while the noise increases with rising temperatures. Next, the fake hit rate was analyzed, showing that it scales with temperature, which is expected, as the lower threshold increases the likelihood of fake hits. Following this, the timing parameters of the encoding were examined. For both chips, the time

delays increased in every parameter due to the use of CMOS logic gates, which exhibit temperature-dependent propagation delays. This leads to changes in the time encoding that need to be taken into account. To explore the digital output pulse shape, the DPTS chips were pulsed, and the influence of temperature on the amplitude and slope was investigated. Since both amplitude and slope increased with temperature, their ratio was analyzed to determine which effect was more prominent. This led to the conclusion that the timing performance slightly improves for the DPTS-X, while remaining relatively stable for the DPTS-O. This results in the need for future detectors to account for the impact of temperature on both noise levels and timing parameters to ensure consistent performance in varying environments.

Lastly, the influence of temperature on the BabyMOSS was analyzed. Similar to the DPTS, the threshold decreases while the noise increases with rising temperatures. Additionally, the number of noisy pixels was investigated, showing that this number also increases with temperature. The fake hit rate of the BabyMOSS was then examined by applying a mask over the noisy pixels and measuring the FHR of the chip. The findings show that the FHR increases with temperature, reaching values as high as $10^{-6}\,\mathrm{pixel}^{-1}\mathrm{s}^{-1}$. That means, that future detector designs should integrate methods to mitigate temperature-induced noise and control the fake hit rate, particularly through masking or adaptive thresholding techniques.

In summary, the performance of all the examined test structures is temperature-dependent, emphasizing the importance of ensuring that the cooling of upcoming detectors is as homogeneous as possible. If uniform cooling cannot be achieved, the discussed effects should be taken into account for the calibration process to ensure consistent tracking performance and uniform efficiency throughout the detector.

For future experiments, one of the main challenges will be to develop an effective cooling system, either to cover large areas, as required for the ALICE3 OT, or to ensure operation in a vacuum, as planned for the ALICE3 IRIS tracker. Specifically, the built setup will be used to characterize the large pitch APTS, which are expected to be produced in the spring of 2025. These characterizations will be crucial for the design of the cooling system for the ALICE3 OT. This work has shown that cooling systems for such detectors can be engineered to operate sensors at temperatures up to 25°C, even under high irradiation, without significant issues.

Acknowledgments

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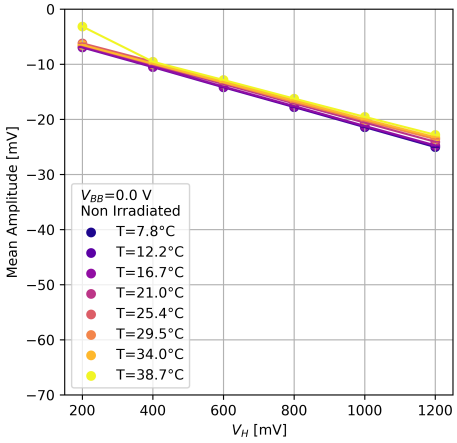
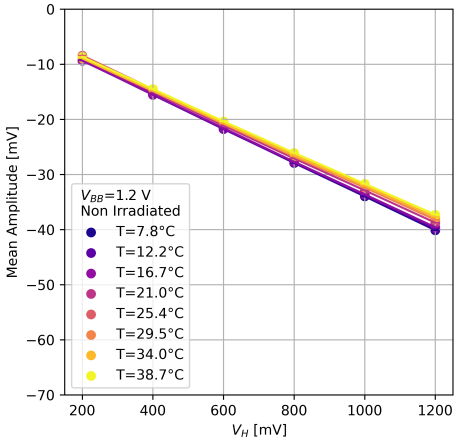
A. Appendix

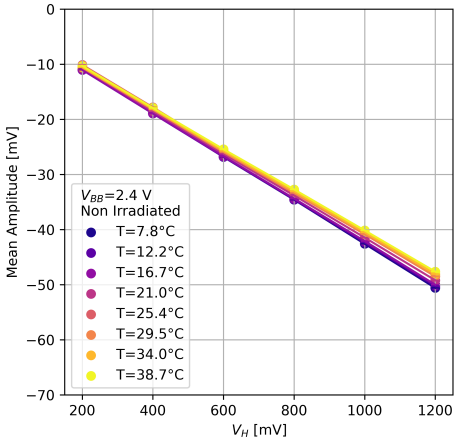
This chapter provides additional figures from the APTS pulsing experiments. While the results are referred to in the main text, the figures are presented here for improved visibility. The plots illustrate the mean amplitude and mean slope of the analog waveforms for the three examined APTS chips, shown as a function of the pulse height V_H, across all tested back biases V_{BB} and temperatures.



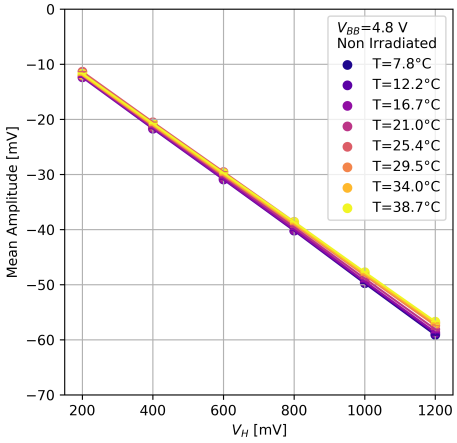
(a) $V_{BB} = 0.0\,\mathrm{V}$



(b) $V_{BB} = 1.2\,\mathrm{V}$

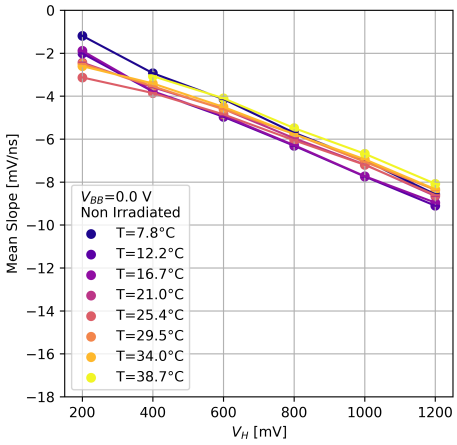


(c) $V_{BB} = 2.4\,\mathrm{V}$

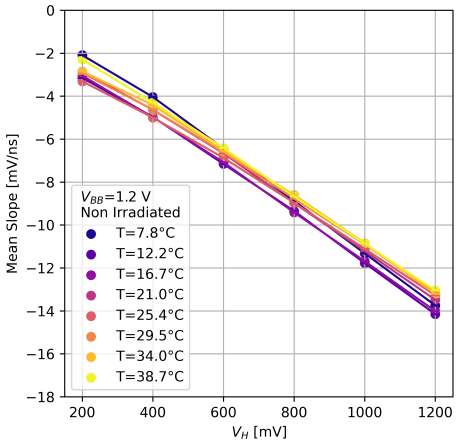


(d) $V_{BB} = 4.8\,\mathrm{V}$

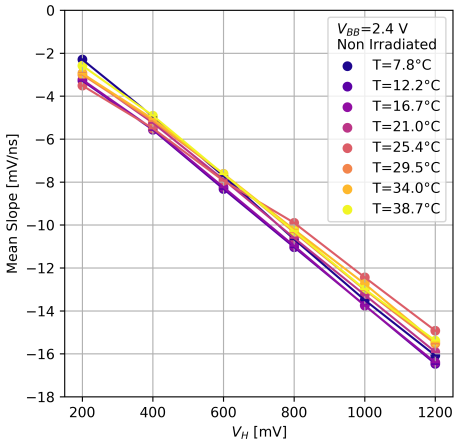
Figure A.1.: The mean amplitude of the non-irradiated chip as a function of V_H for the different back biases and temperatures.



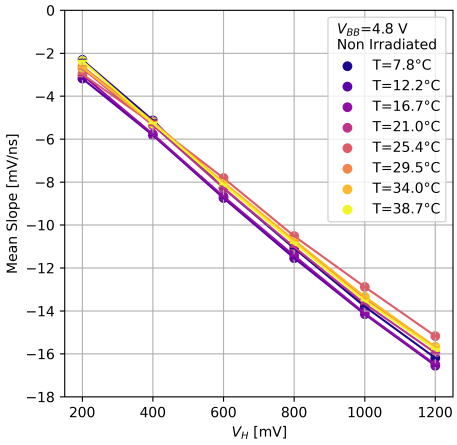
(a) $V_{BB} = 0.0\,\mathrm{V}$



(b) $V_{BB} = 1.2\,\mathrm{V}$

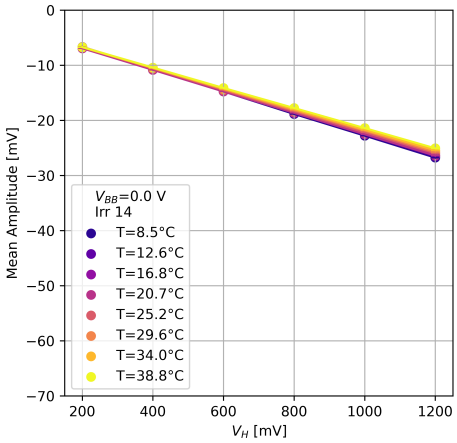


(c) $V_{BB} = 2.4\,\mathrm{V}$

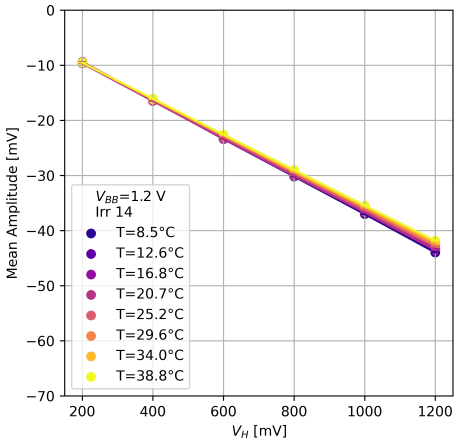


(d) $V_{BB} = 4.8\,\mathrm{V}$

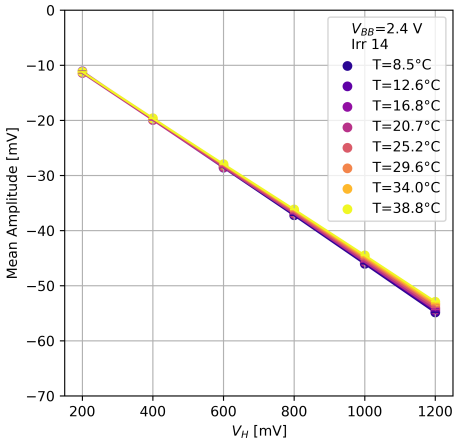
Figure A.2.: The mean slope of the non-irradiated chip as a function of V_H for the different back biases and temperatures.



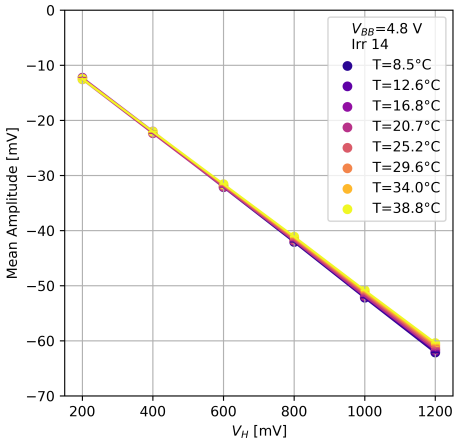
(a) $V_{BB} = 0.0\,\mathrm{V}$



(b) $V_{BB} = 1.2\,\mathrm{V}$

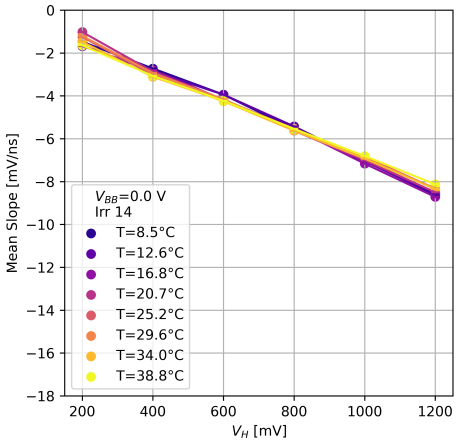


(c) $V_{BB} = 2.4\,\mathrm{V}$

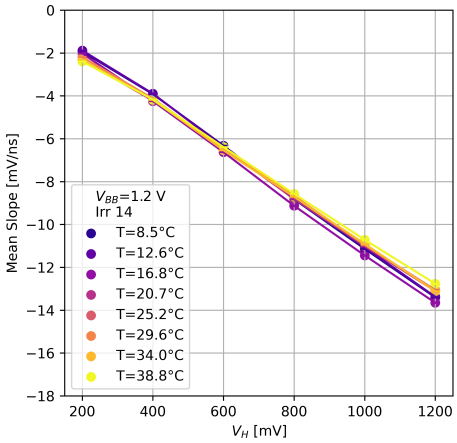


(d) $V_{BB} = 4.8\,\mathrm{V}$

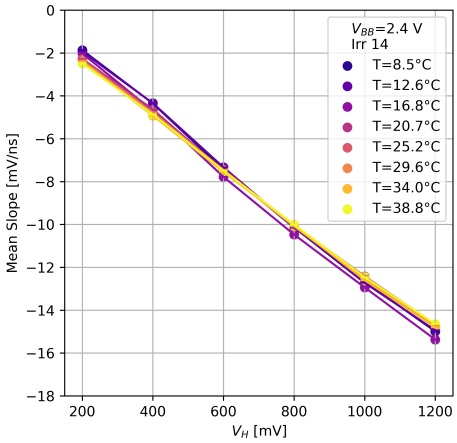
Figure A.3.: The mean amplitude of the $10^{14}\,\mathrm{MeV\,n_{eq}\,cm^{-2}}$ irradiated chip as a function of V_H for the different back biases and temperatures.



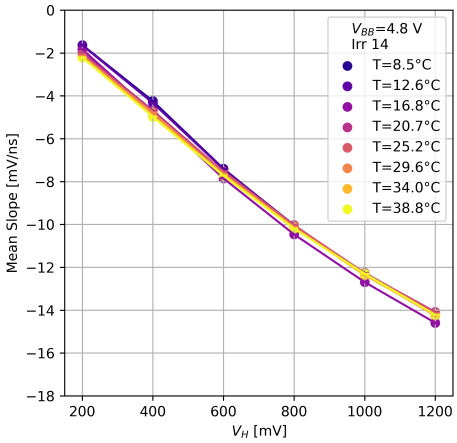
(a) $V_{BB} = 0.0\,\mathrm{V}$



(b) $V_{BB} = 1.2\,\mathrm{V}$

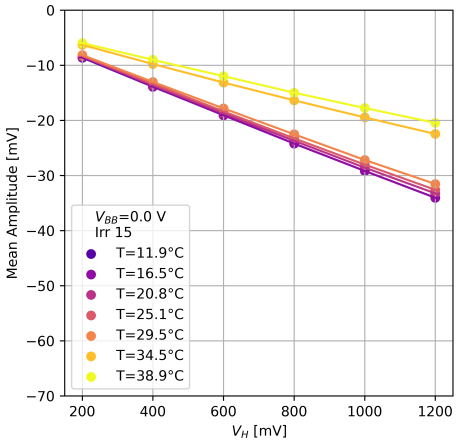


(c) $V_{BB} = 2.4\,\mathrm{V}$

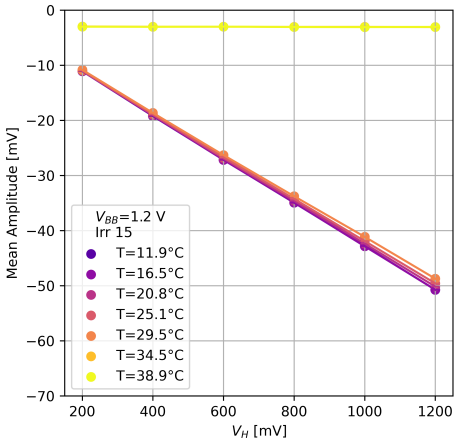


(d) $V_{BB} = 4.8\,\mathrm{V}$

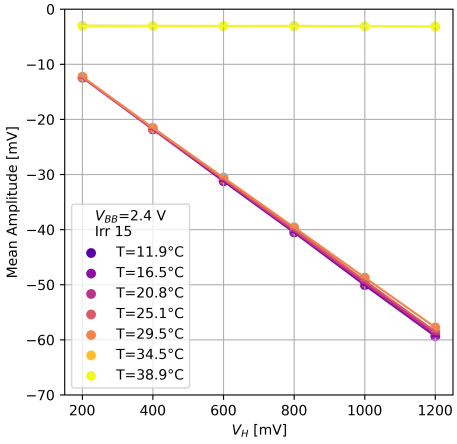
Figure A.4.: The mean slope of the $10^{14}\,\mathrm{MeV\,n_{eq}\,cm^{-2}}$ irradiated chip as a function of V_H for the different back biases and temperatures.



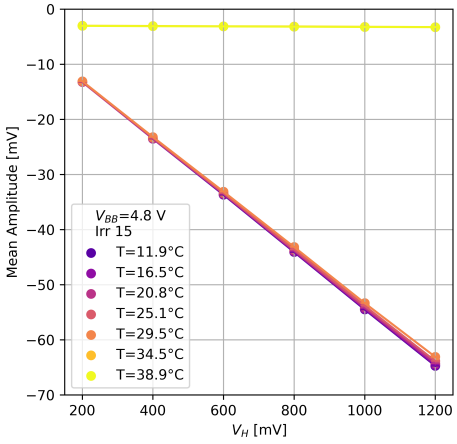
(a) $V_{BB} = 0.0\,\mathrm{V}$



(b) $V_{BB} = 1.2\,\mathrm{V}$

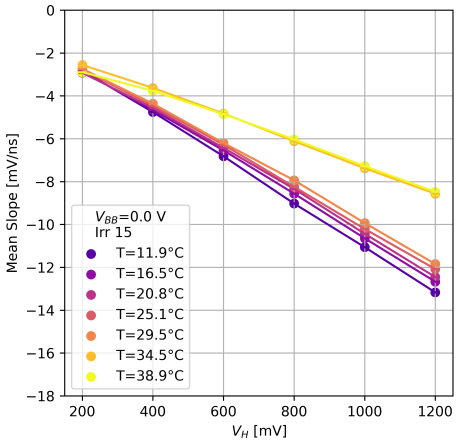


(c) $V_{BB} = 2.4\,\mathrm{V}$

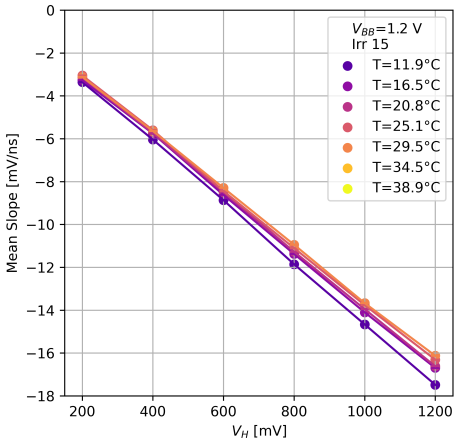


(d) $V_{BB} = 4.8\,\mathrm{V}$

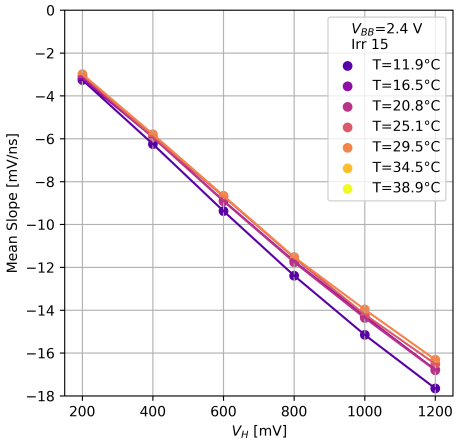
Figure A.5.: The mean amplitude of the $10^{15}\,\mathrm{MeV\,n_{eq}\,cm^{-2}}$ irradiated chip as a function of V_H for the different back biases and temperatures.



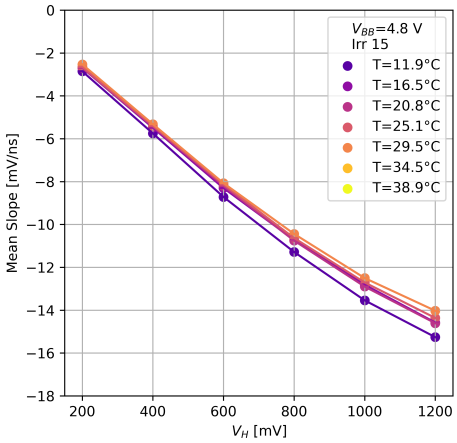
(a) $V_{BB} = 0.0\,\mathrm{V}$



(b) $V_{BB} = 1.2\,\mathrm{V}$



(c) $V_{BB} = 2.4\,\mathrm{V}$



(d) $V_{BB} = 4.8\,\mathrm{V}$

Figure A.6.: The mean slope of the $10^{15}\,\mathrm{MeV\,n_{eq}\,cm^{-2}}$ irradiated chip as a function of V_H for the different back biases and temperatures.