Technische Universität München
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Bachelor Thesis in Physics

Development of a cooling system for a silicon particle detector

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Introduction

The **H**igh **A**cceptance **D**i-**E**lectron **S**pectrometer (HADES) is a fixed target experiment located at SIS18[1] operated by the GSI[2] in Darmstadt. The maximum kinetic beam energy for SIS18 is 1 AGeV for heavy ions, 2 AGeV for ions and 4.5 GeV for protons. HADES contains several subsystems for particle identification, momentum and energy loss measurements. The spectrometer geometry is organized in six sectors and covers 85% of azimuthal angle between 18° and 85° (Fig. 1).

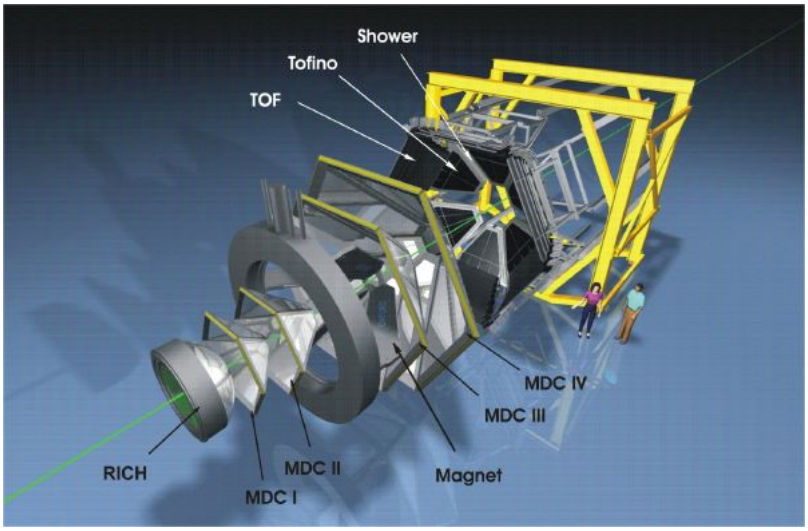

Figure 1: Exploded view of the HADES spectrometer located at the GSI in Darmstadt.

The HADES physics program covers lepton and hadron physics in elementary and heavy ion collisions. One aim is to study elementary processes, especially the creation of light vector mesons, as a comparison for in-medium processes that should occur when colliding heavy ions. These elementary processes are induced by pions, protons or deuterons on solid or liquid targets. Big emphasis lies on studying in-medium properties of the mesons where the width and mass could be modified in dense and hot nuclear matter. Vector mesons are examined in normal nuclear matter, light projectiles (protons, pions) on heavy ion targets, as well as in nuclear matter with high densities ($\rho = 2 - 3\ \rho_0$) and moderate temperature ($T = 90$ MeV). Here the mesons act like a probe of the dense nuclear matter phase, due to the fact that some mesons decay in the same time

[1] Synchrotron - heavy ion synchrotron, 18 denotes maximum bending power 18 Tm

[2] GSI Helmhotzzentrum für Schwerionenforschung

frame as the fireball of collision exists. Especially the rare decay channel of light vector mesons into an e^-/e^+ pair is of great interest, because they are not influenced by strong forces. Dense nuclear matter is generated by shooting relativistic heavy ions on heavy ion targets. Another advantage by doing so is the creation of particles due to secondary reactions. Some of these other particles include strangeness which is for great interest in our group.[3]

1 The HADES spectrometer

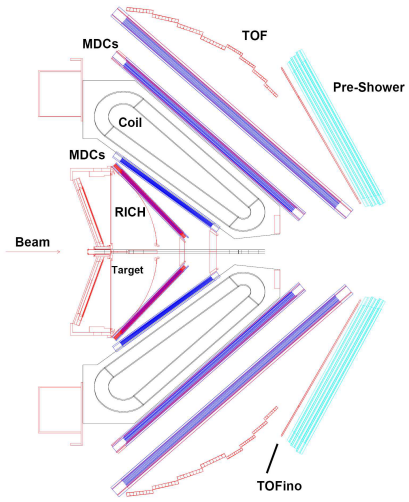

Figure 2: Schematic arrangement of the detectors that compose the HADES spectrometer. The first detector is the Ring Imaging Cherenkov detector (RICH), following up the MDCs for particle identification. Afterwards the Multiplicity and Electron Trigger Array (META) that consists of the two time-of-flight detectors (TOF, TOFINO) and PreShower detector. Meanwhile the TOFINO was replaced by Resistive Plate Chambers (RPCs).

HADES has a 6-folded azimuthal symmetry with a fixed target. The target is inside the Ring Imaging Cherenkov (RICH) gas detector used for e^-, e^+ identification. The RICH is a hadron blind detector due to the requirement of $\beta > 0.85$[3] for Cherenkov radiation emission. Hadrons have β below 0.85. The RICH is followed by two sets of Multiwire Drift Chambers (MDC). The MDCs are located before and after a toroidal magnet which bends trajectories of charged particles. Through the four hits in the MDCs it is possible to reconstruct the deflection angle and so the momentum of the particles. Besides that the MDCs measure the $\mathrm{d}E/\mathrm{d}x$. Afterwards there are two Time-of-Flight detectors: TOFino and TOF. Both consist of plastic scintillators which measure the velocity of the traversing particles. Particles could be identified via the momentum extracted from fitting the trajectories in the magnetic field or $\mathrm{d}E/\mathrm{d}x$ information of the MDCs and the velocity information of the TOF/TOFino. The PreShower wall is placed behind the TOFino and is made up of two lead converter arranged between three wire chambers. The electromagnetic showers are produced by leptons that cause Bremsstrahlung and pair production in the detector. TOF, TOFino and PreShower build up the Multiplicity and Electron Trigger Array (META).
In 2009-2010 the HADES spectrometer was upgraded to enable more precise measurements with heavy ions. The TOFino was replaced by Resistive Plate Chambers (RPCs) that provide an improved time resolution of about 100ps. The combination of TOF and

[3] For this specific detector. In general $\beta > 1/n$, n is the refraction index of the radiation medium.

the RPCs offers HADES the possibility to cover multiplicities of up to 200 charged particles per event in heavy ion collisions.[3][4]

One of the next propositions at the HADES spectrometer is to collide pions with nuclear targets. An aim is to study the interaction between nuclear matter and strange mesons like K_s^0. Besides that it is planned to measure strange bayrons like $\Sigma(1385)$ and $\Lambda(1405)$ with high precision. One advantage of the pion beam is that they transfer only a low momentum, due to their low mass, to the produced vector mesons. Theses vector mesons decay already in the medium and provide much better information about in-medium modifications.

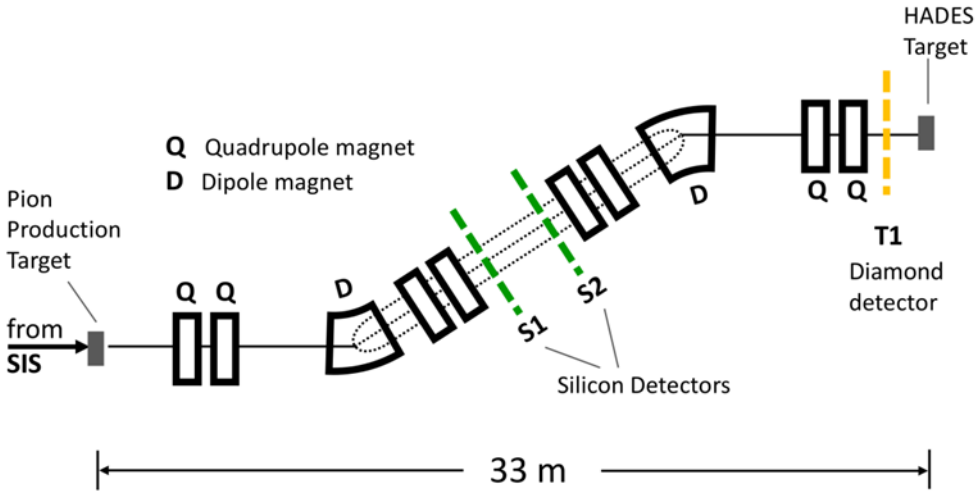

Figure 3: An overview of the pion beam tracking system, CERBEROS, which consists of two silicon detectors that are located at S1 and S2, and a diamond detector at T1. The quadrupole (Q) and dipole (D) magnets are used for focussing and bending the pion beam.

Due to the fact that the pion beam is a secondary beam, the pion momentum is spread up to 10% around the central beam momentum p_c. As the precise knowledge of the pion momentum is important for the exclusive analysis, we have to measure the momentum of the pions precisely. For this purpose a pion beam tracking system called CERBEROS is developed. CERBEROS consists of two silicon detectors, which are located after the production target between two quadrupole magnets in the beam line. Both detectors have to be radiation hard to cope the high-intensity secondary beam. Cooling a silicon detector strongly improves the radiation-hardness and performance. It reduces the leakage current, and thus the noise. Moreover the harmful reverse annealing process can be reduced or totally suppressed. That is why effective detector cooling is crucial for the operation of this detector.

1 Principle of silicon detectors

1.1 Properties of intrinsic silicon

Silicon is a semiconductor with a band gap energy of about $E_g = 1.12$ eV. Due to the indirect band gap of silicon, an energy of 3.4 eV is needed to create an electron-hole pair. These electron-hole pairs are already created at room temperature. Moreover silicon has a high density. The combination of high density and relatively small energy, to create an electron-hole pair, causes a huge number of charge carriers, that are introduced by through going ionizing particles. Another advantage is the fast charge collection time ($\sim$ 10 ns), because charge carriers can move nearly free inside silicon.[10]

1.2 Extrinsic silicon

In an intrinsic semiconductor electrons and holes are only generated pairwise due to thermal excitation. By adding impurities inside the crystal lattice (doping) properties are changed. In an n-type silicon, the impurities are called donors (e.g. phosphorus), because they have one extra valence electron. Donors thermally release their electron into the conduction band, leading to more electrons in the conduction band than holes in the valence band. In this case the electrons are called majority charge carriers. Contrary to that in p-type silicon, the added impurities are called acceptors (e.g. boron) and have one valence electron less. Here the holes are the majority and electrons the minority charge carriers.

1.3 p-n junction

A p-n junction is produced by connecting two extrinsic semiconductors with the opposite doping. Electrons from the n-region and holes from the p-region recombine in the junction area. This space-charge region is called depletion zone. Positively charged ionized donors in the n-type material and negatively charged ionized acceptors in the p-type material are left behind, building up a potential difference. The charged acceptors and donors attract the minority charge carriers leading to a drift current. The majority carriers diffuse in the opposite direction through the junction. In thermal equilibrium the diffusion current of the majority carries and the drift current cancel out, there is

no net current flow. A depletion zone is not only created at p-n junction, n^+-n or p^+-p junctions can also produce a space-charge region.

By applying a positive potential at the p-side, the junction is forward biased and a net current flows. The junction is reverse biased, if a negative potential is applied at the p-layer, causing an increase of the depletion zone size. If an ionizing particle transverses the depletion zone, electrons and holes are created. These are extracted in opposite directions by the electric field such that they can not recombine. For the operation of silicon detectors it is essential to prevent charge carriers, electrons and holes, from recombining, because the at the electrodes collected charge carriers generate the signal for the read out.[10][8]

1.4 Silicon detector

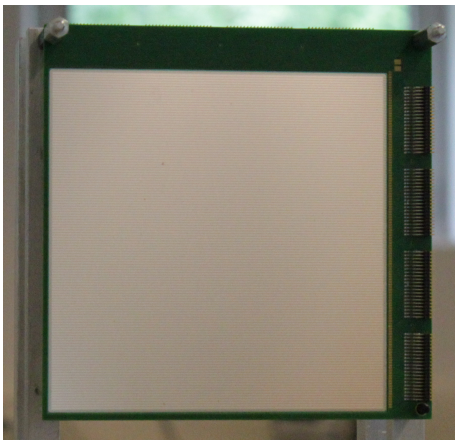

Figure 1.1: Picture of the silicon detector, which is part of the pion beam tracking system, CERBEROS.

The silicon strip detector which is part of CERBEROS has an active area of 100×100 mm^2. The silicon wafer is 300 μm thick and glued[1] on a PCB[2], which in our case is only made out of FR4[3]. The quadratic PCB ($l = 114.1$ mm) is 2.2 mm thick. For a two dimensional position resolution the detector is double sided with strips on both sides which are perpendicular to each other. In total the readout is composed of 2×128 strips.
The bulk is p-type with a highly doped n-layer to ensure a large depletion zone in the detector. On the other side is a highly doped p-layer, which makes the detector radiation hard.

[1] Glue: KJR 9022E (Shinetsu)
[2] PCB: Printed Circuit Board
[3] Material composed of epoxy resin

2 Radiation damage

There are two types of damage caused by radiation. One is the surface damage due to ionizing energy loss and the other one is the bulk damage due to Non Ionizing Energy Loss (NIEL). The bulk damage will be discussed in the following. Bulk damage is introduced by dislocation of a single atom from its position in the lattice. The dislocation of an atom creates a interstitial-vacancy pair, which is called Frenkle pair. [8]

2.1 Primary defects and secondary defects

The minimum energy to displace an atom from its lattice side is around 25 eV. Recoil energies roughly below 1–2 keV can only create isolated (single) defects. For recoil energies between 2–12 keV the Primary Knock on Atom (PKA) is able to create additional Frenkel pairs and it is also possible that one defect cluster is formed. If the energies are even higher several clusters and point defects can be created. It is also possible that the primary defects, interstitials and vacancies, diffuse at room temperature through the crystal and build up clusters.[8][7]

2.2 Formation of energy levels within the band gap

Clusters created due to radiation damage can form additional energy levels within the forbidden band gap, that have different electrical properties.
Such clusters can act like recombination-generation centres, they can easily capture and emit electrons and holes due to thermal excitation. These energy levels lie close to the middle of the band gap.
Other clusters behave like trapping centres. Electron and holes are captured and emitted after some time delay depending on the depth of the energy level. The capturing of electrons and holes reduce the signal. Beyond that, the signal can also be increased when electrons and holes from previous events are released.
They also may change the space charge in the space-charge region, which increases the needed bias voltage.[8][10]

2.3 Beneficial and reverse annealing

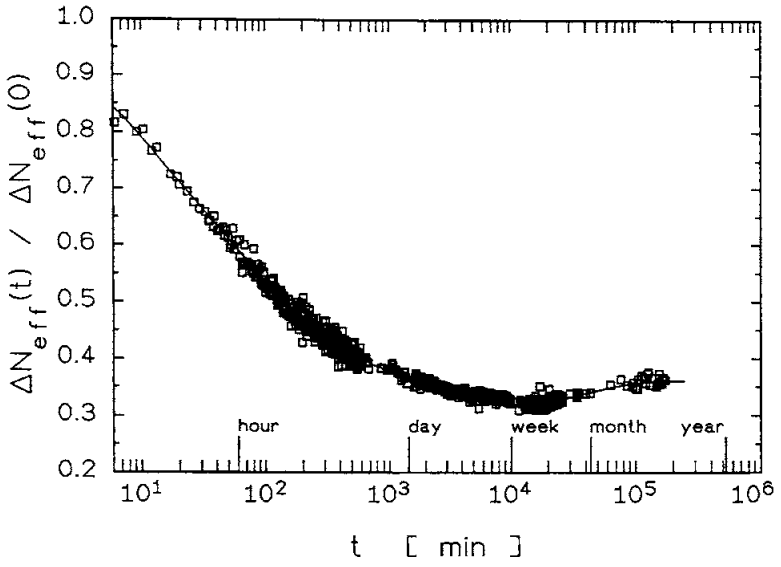

Figure 2.1: Annealing of radiation introduced changes of effective doping concentration at $T = 20°C$, after short irradiation and long term observation.[13]

Primary defects are not stable. Interstitials and vacancies are mobile at room temperature causing partially annealing of defects. This effect is called beneficial annealing. In most cases this means only that defects change their properties and turn from electrically active to non-active. The crystal lattice becomes only perfect again when an interstitial recombines with a vacancy. Though there exists also reverse annealing where primary defects build up stable electrically active clusters. Both annealing effects are strongly temperature depended but have different time constants ($\tau(T)$).

Beneficial annealing happens mostly shortly after irradiation, in the time scale of weeks at room temperature.

$$N_d = N_d(0) \cdot e^{-t/\tau}, \tau(T) \propto e^{E_a/(kT)} \tag{2.1}$$

,where $N_d(0)$ is the number of defects with a characteristic property which exist right after irradiation and E_a is the activation energy for a particular defect to migrate through the crystal. $\tau(T_{ann})$ is of the order of 10 min. Every kind of defect is stable blow its "annealing temperature" (T_{ann}).

Reverse annealing dominates in time scale of months at room temperature. There are two different mechanism that cause electrically active defect complexes. On one hand electrically inactive defects could decay into active ones. On the other hand can two electrical inactive clusters react with each other an become electrically active. The change in the number of defects due to reverse annealing is described by:

$$N_Y(\phi, t, T) = N_{Y_\infty}(\phi) \cdot \left(1 - \frac{1}{1 + N_{Y_\infty}\tilde{k}(T)t}\right) \tag{2.2}$$

,where $\tilde{\mathrm{k}}$(T) is the inverse of the time constant of the reverse annealing ($\tilde{k}(T) = 1/\tau$) and N_{Y_∞} is the concentration of defects due to irradiation.

Cooling slows down beneficial and reverse annealing. With temperatures below approximately 0°C reverse annealing is completely suppressed while beneficial annealing still occurs. Furthermore N_{eff} is relatively stable below temperatures of -10°C. The operation temperature is always a compromise between beneficial and reverse annealing. Cooling is important not only for the detector performances during the exposure high radiation intensities, it is also important in non operation times.[8][7]

2.4 Change of the effective doping

The creation of defects inside the lattice could lead to the removal of original donors and acceptors (dopants). If phosphorus combines with a vacancy, it looses his functionality as a donor and becomes neutral. Defect complexes can also create effective donors and acceptors inside the depletion zone. The change in the effective doping concentration is described by:

$$N_{eff}(\phi) = N_{D,0}e^{-c_D\phi} - N_{A,0}e^{-c_A\phi} + b_D\phi - b_A\phi \tag{2.3}$$

$N_{D,0}, N_{A,0}$ are the donor and acceptor concentration before irradiation. c_D, c_A, b_D, b_A are constants, which have to be experimentally determined. $b_D\phi$ describes the removal of donors and $b_A\phi$ the removal of acceptors.

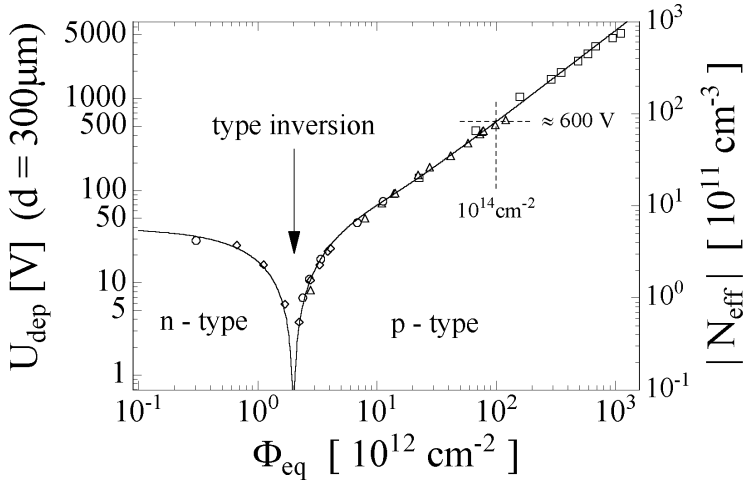

Figure 2.2: Fluence dependence of the magnitude of effective doping for n-type silicon wafer irradiated with 1 MeV neutrons equivalent. The data have been corrected for self-annealing occurring already during the extended irradiation period. Also shown is the much smaller effect of irradiation with 1.8 MeV electrons also scaled to 1 MeV neutron equivalent NIEL.[13]

Irradiation introduces mainly acceptor-like defects within the bulk, leading to a change in the effective doping concentration. After irradiation n-type becomes intrinsic and then more and more effectively p-type. This effect is called type inversion (see Fig. 2.2). It only occurs by n-type, p-type gets only more doped.[8]

The change in the effective doping concentration shifts the depletion voltage V_{fd}, since:

$$V_{fd} \approx \frac{e}{2\epsilon_0\epsilon_r}|N_{eff}|d^2 \tag{2.4}$$

e is the elementary charge, $\epsilon_0\epsilon_r$ are the permittivity of the material, N_{eff} is the effective doping concentration and d is the width of the depletion zone.[7]

2.5 Leakage current

The leakage current is strongly temperature dependent due to thermal excitation. Generation centres that are responsible for the creation of leakage current I, lie close to the middle of the band gap.

$$I = T^2 \cdot e^{-\frac{E}{k_B T}} \tag{2.5}$$

For an unirradiated silicon wafer is E the band gap energy E_g with a value of about 1.12 eV. But this value of E changes after irradiation. Normally the current is compared to the current at room temperature (20°C). The leakage current can be enormously reduced by cooling, e.g. $I(-10°) = 0.064 \cdot I(20°)$. Cooling is crucial, because an increase

of the leakage current causes local heating, and thus an increase of leakage current. This effect is called thermal runaway.[11][2][1]

Radiation introduced change in the leakage current can be described using the NIEL hypothesis that scales the damage defects caused by different particles:

$$\Delta I = \alpha(t,T) \cdot \Phi_{eq} \cdot V \tag{2.6}$$

V is the depletion volume. $\alpha(t,T)$ is called current related damage rate. It is dependent on the time t between the exposure of radiation and the current measurement just as the operation temperature due to the fact that some defects anneal. $\alpha(t,T)$ is nearly material independent.

Φ_{eq} is the integrated equivalent flux. It is a normalization to the flux of 1 MeV neutrons that is used instead of the integrated flux of a particular particle.

$$\Phi_{eq} = \kappa \cdot \Phi \tag{2.7}$$

κ is the ratio of the irradiation damage caused by a particular particle and 1 MeV neutrons.

$$\kappa = \frac{\int D(E)\Phi(E)\mathrm{d}E}{D_{neutrons}(E = 10MeV)\int \Phi(E)\mathrm{d}E} \tag{2.8}$$

D(E) is the cross section for dislocation, $D_{neutrons}(E = 10\text{ MeV}) = 954$ MeVmb,:

$$D(E) = \sum_v \sigma_v(E) \int_0^{E_R} f_v(E, E_R)P(E_R)\mathrm{d}E_R \tag{2.9}$$

σ_v is a cross section and v are all possible reactions leading to dislocation of lattice atoms. E_R is the recoil energy of the Primary Knock on Atom (PKA). $f_v(E, E_R)$ is the probability to produce a PKA with a recoil energy E_R when the incoming charged particle has an energy E. $P(E_R)$ is the Lindhard probability. If the recoil energy E_R is below the minimum energy to displace an atom ($E_{d,min} = 25$ eV) the probability $P(E_R)$ is zero.[7]

3 Development of a cooling device

According to the results of last beam time, the silicon detector has to be operated at a temperature below 0°C. A temperature of -10°C would be optimal. The design of the cooling system is done with SolidWorks. To improve the design several thermal and statical analysis are accomplished using Finite Element Method (FEM).

The cooling devices are designed such to fit into the beam pipe and not to interfere with the read-out electronics.

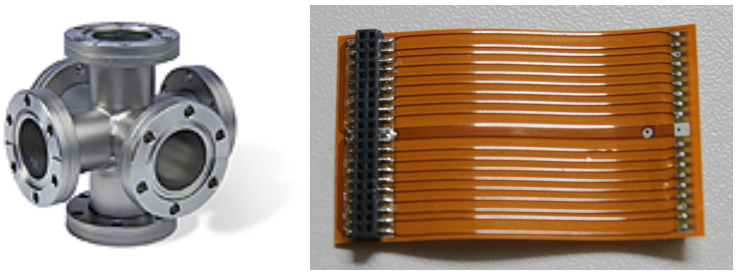

Figure 3.1: *left*: 6-way vacuum cross *right*: junction cable of the electronics.

3.1 Finite Element Method

FEM divides complex shapes into several small elements. These elements are characterized through points called nodes that are connected to each other spanning a grid called mesh that holds the element together. The field strength of the whole element is interpolated by a set of simultaneous polynomial equations at the nodes. Connected nodes of bordering elements share the same degrees of freedom (DOF). The polynomial equations are only an approximation of partial differential equations (PDE) that describe physical phenomena, because it is nearly impossible to solve PDE with analytical methods for complex shapes. The polynomial equations are solved iteratively until the condition of equilibrium is reached.[12][5]

3.2 Indirect cooling via PCB

First of all we tried to cool down the silicon wafer without direct contact to the cooling device. Every direct contact to the wafer could damage the wafer.

3.2.1 Boundary conditions

To ensure a precise momentum measurement the detector is located in a vacuum pipe. There are only two ways to exchange heat, namely through the direct connection of solids, and through heat radiation. The Front-End electronics are located on the outside of the detector, causing no a additional heat. Heat is only produced by the the leakage current ($\sim$ 2 μA) in combination with the depletion voltage (110 V) and also by the energy deposit of the pions. The energy loss of a MIP in 300 μm silicon is about 160 keV. The worst case would be that all 10^8 beam particles/s lose 10 MeV of their energy. The number of particles can still change, because the position of the detector is not yet defined. All together the silicon wafer is exposed to a heat source of 380 μW.

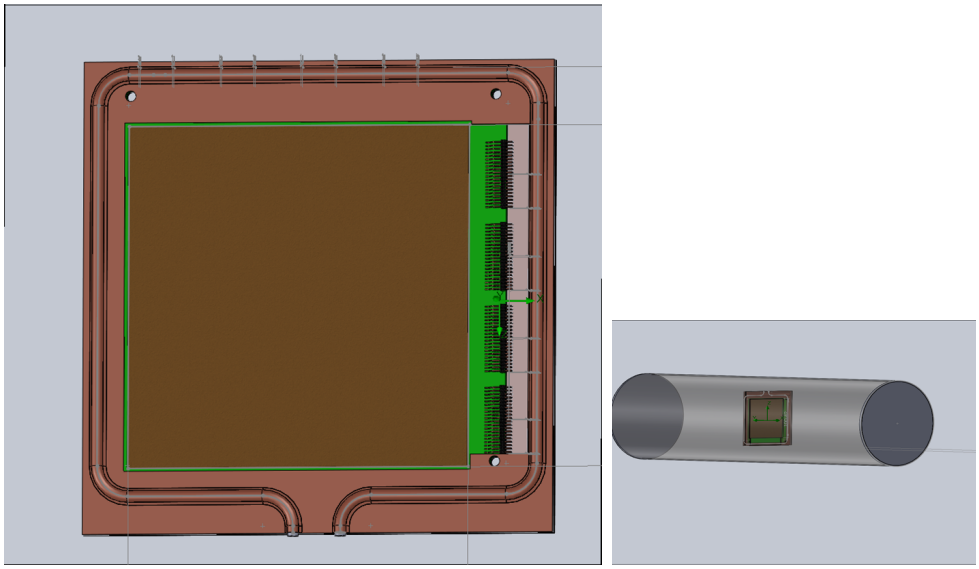

Figure 3.2: *left*: CAD picture of the cooling device *right*: cooling device located in vacuum pipe.

The cooling device consists of two square copper boards (l = 139 mm, d = 1 mm). The plates were cut in such a manner that the active area of the wafer and the electronic readout remains uncovered. There is a copper pipe for the cooling solvent (d_{outer} = 3.4 mm, d_{inner} = 3 mm) soldered to the upper copper panel. To guarantee a cooling from both sides the copper boards are connected by a rectangular piece of copper (l_1 = 8 mm, l_2 = 135 mm, d = 2.2 mm). The Cu boards on either side are lying directly on the PCB without contact to the silicon wafer. The circuit paths of the electronic readout on the detector are not taken into account in the simulation.
In the first thermal simulation Propan is used as a cooling fluid, set at a temperature of

-20°C with a mass flow of 0.001 kg/s. Most cryothermostats are unable to cool fluids down, below a temperature of -25°C. The glue between the silicon wafer and the PCB is included as a thermal resistance ($\lambda = 0.18$ W/mK, $d = 100$ μm). Furthermore the heat source (380 μW) is part of the simulation. The outside of the vacuum pipe is set at room temperature (20°C). Heat radiation is exchanged between all parts of the model.

	Si	PCB	Cu	stainless steel
ϵ	0.92	0.9	0.02 - 0.03	0.5

Table 3.1: Emissivity of the materials included into the simulation

3.2.2 Results of thermal simulations

The figure below (Fig. 3.3) shows the temperature distribution on the detector. As one can see the temperature distribution on the silicon wafer is rather homogeneous but with an average temperature between $1.5 - 4.5$°C from the temperature scale and therefor to high.

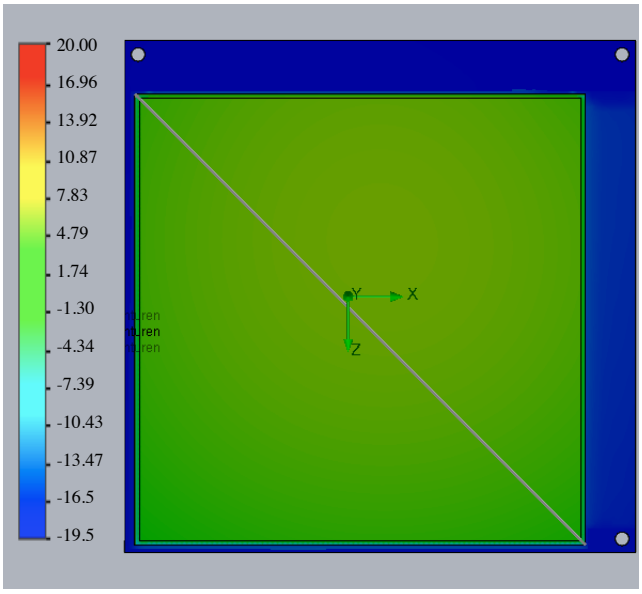

Figure 3.3: CAD picture of the temperature dispersion on the detector as a result of the cooling with the indirect cooling device with glue and heat source included in the simulation.

The temperature of the silicon wafer as a function of the position along a diagonal (Fig. 3.3: grey line) is shown in Fig. 3.4. The temperature of the outer faces rises immediately, because of the bad heat transfer from PCB to silicon. Furthermore the maximum value of the temperature gradient is at $\sim 5°C$ in the middle of the wafer.

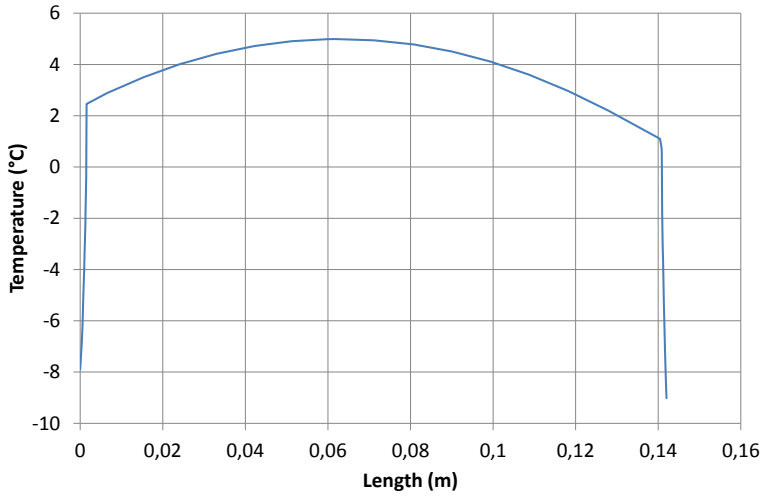

Figure 3.4: Temperature gradient along a diagonal (Fig. 3.3: grey line) through the silicon wafer as a result of the cooling with the indirect cooling device with glue and heat source included in the simulation.

	Minimum	Maximum	Average
silicon wafer	0.31°C	5.16°C	3.83°C
PCB	-19.02°C	3.24°C	-16.97°C

Table 3.2: Temperature, if glue and heat source are taken into account.

Thermal losses through the PCB are significant and caused by the low heat conductivity ($\lambda = 0.3$ W/(mK)) and the high absorption of heat radiation of silicon ($\alpha = 0.92$). The temperature gradient of the wafer is $\Delta T = 5.37°C$.

In the next simulation the glue is not included to examine how much the glue influences the temperature of the silicon wafer, because it was not possible to obtain all specific material properties that are necessary to integrate the glue properly into the CAD model of the detector.

Figure 3.5 shows that the temperature distribution stays homogeneous, but the temperature is lower with a value of about $T_{mean} = 0°C$, which indicates that the glue has a not negligible influence on the heat conduction between PCB and silicon wafer.

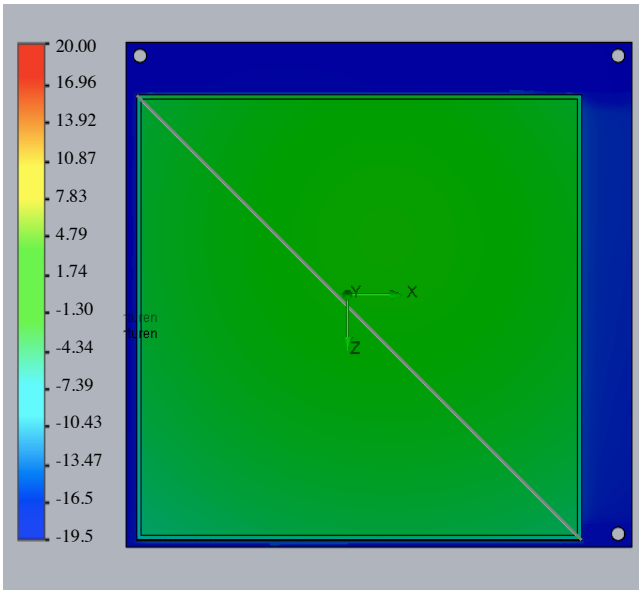

Figure 3.5: CAD picture of the temperature distribution on the detector as a result of the cooling with the indirect cooling device, if heat source is included and the glue is not taken into account.

In Fig. 3.6 the temperature is again plotted against the length of a diagonal on the silicon wafer (see Fig. 3.5: grey line). The gradient of the temperature behaves the same like in Fig. 3.4, but is shifted to lower temperatures. The maximum value of the temperature in Fig. 3.4 is around 5°C and below 1°C in this plot (Fig. 3.6).

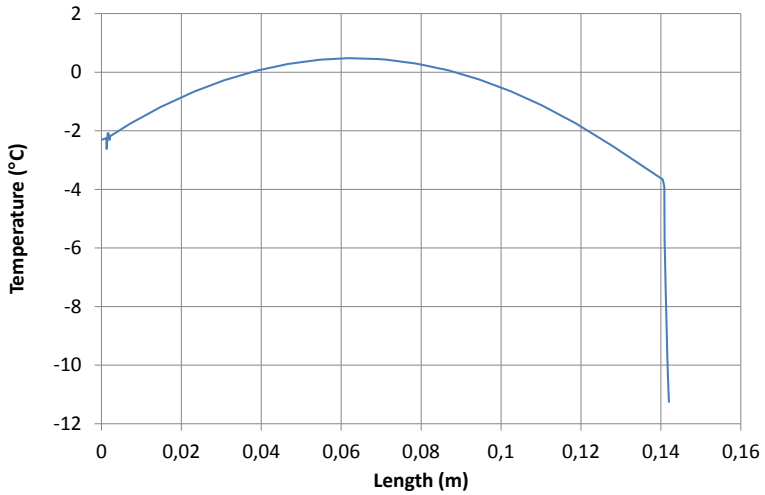

Figure 3.6: Temperature gradient along a diagonal (Fig. 3.5: grey line) through the silicon wafer as a result of the cooling with the indirect cooling device, if heat source is included and glue is not taken into account.

	Minimum	Maximum	Average
silicon	-4.63°C	0.7°C	-0.78°C
PCB	-19.16°C	-0.27°C	-17.36°C

Table 3.3: Temperature, if heat source is taken into account and the glue is neglected.

The temperature of the silicon wafer is higher, if the glue is part of the simulation. The glue has a great influence on the temperature and can not be neglected. According to Table 3.2 and 3.3 the difference of the average temperature in the silicon wafer is huge ($\Delta\ T_{average} = 4.62$°C). From now on well estimated values for the glue are used which slightly overpredict its values.

In the following simulation it is investigated how much the silicon wafer is heated up due to the heat source. Therefor the result of the first simulation, in which the glue and the heat source where included, is compared with this simulation, in which the heat source is not taken into account.

As one can see the temperature dispersion is still homogeneous. Moreover there is no significant difference between the temperature dispersion of Fig. 3.3 and Fig. 3.7, because temperature of the silicon wafer is also around 1.74°C.

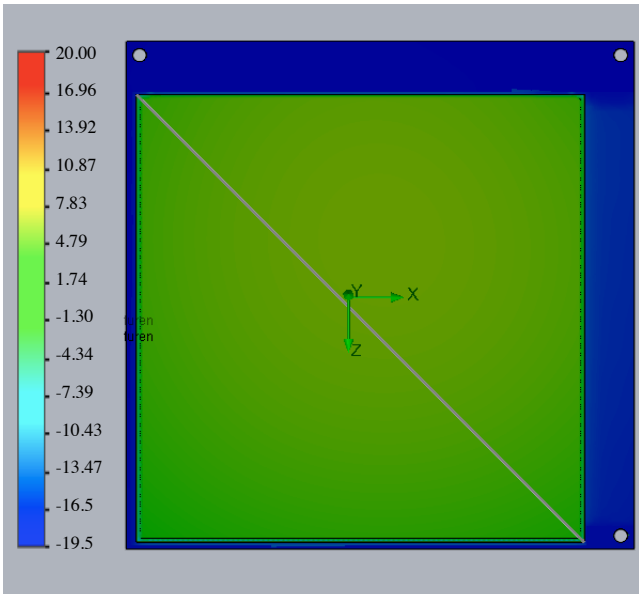

Figure 3.7: CAD picture of the temperature distribution on the detector as a result of the cooling with the indirect cooling device, if glue is included and heat source is not taken into account.

Comparing the temperature gradient along the diagonal of Fig. 3.4 with this figure (Fig. 3.8) there is no considerable difference. Both maximal values are around 5°C. The figures denote that influence of the heat source on the temperature of the silicon wafer is negligible.

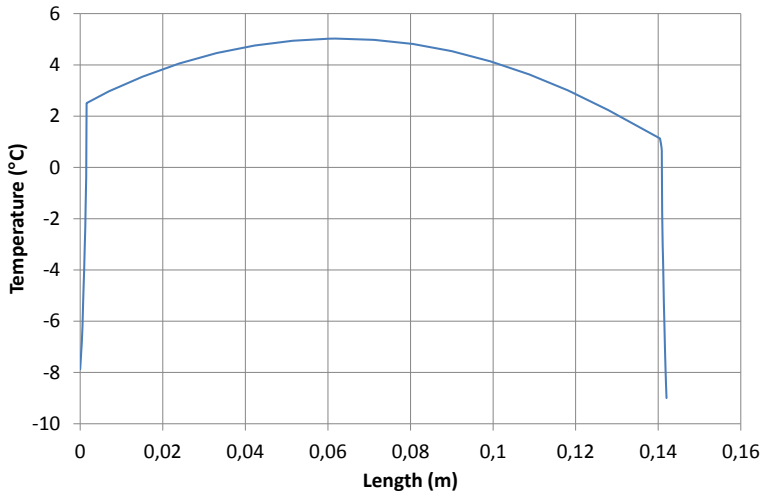

Figure 3.8: Temperature gradient along a diagonal (Fig. 3.7: grey line) through the silicon wafer, if glue is included and heat source is not taken into account.

	Minimum	Maximum	Average
silicon wafer	0.35°C	5.2°C	3.86°C
PCB	-19.02°C	3.26°C	-16.97°C

Table 3.4: Temperature, if glue is taken into account and the heat source is neglected.

One can see that the contribution from the heat source is negligible, comparing Table 3.2 with Table 3.4 ($\Delta T_{silicon} = 0.3 - 0.4$°C and $\Delta T_{PCB} = 0 - 0.02$°C) and will be neglected in the following simulations.

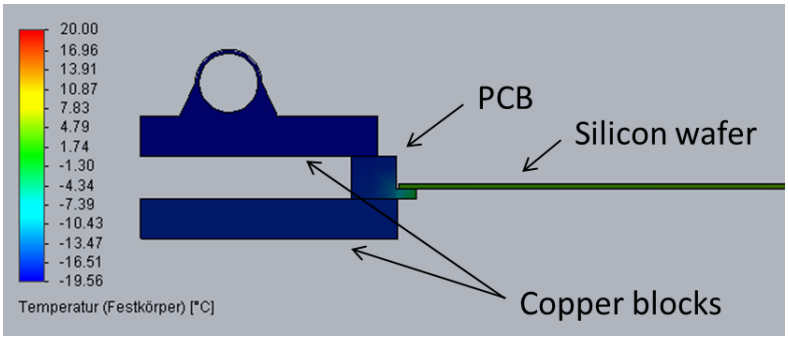

Figure 3.9: CAD cross section view of the temperature distribution of the detector and cooling device.

All in all the cooling through the PCB is insufficient. The copper plates do not cover the whole surface of the PCB. Shortly after the the PCB surface is uncovered, the PCB heats up due to heat radiation (see Fig. 3.9). Furthermore the cooling power is transported poorly to the silicon wafer. Therefor the silicon wafer is only slightly cooled down ($T_{average,silicon} = 3.83°C$). Besides that the temperature difference ($\Delta T_{average,silicon,PCB} = 20.8°C$) is critical because of different heat expansion coefficients of the materials, which can introduce mechanical stress on the silicon wafer.

3.3 Direct cooling via silicon wafer

Considering the results of the previous shown simulation, in the case of the indirect cooling of the detector, the option of a direct cooling of the wafer was considered and tested.

3.3.1 Boundary conditions

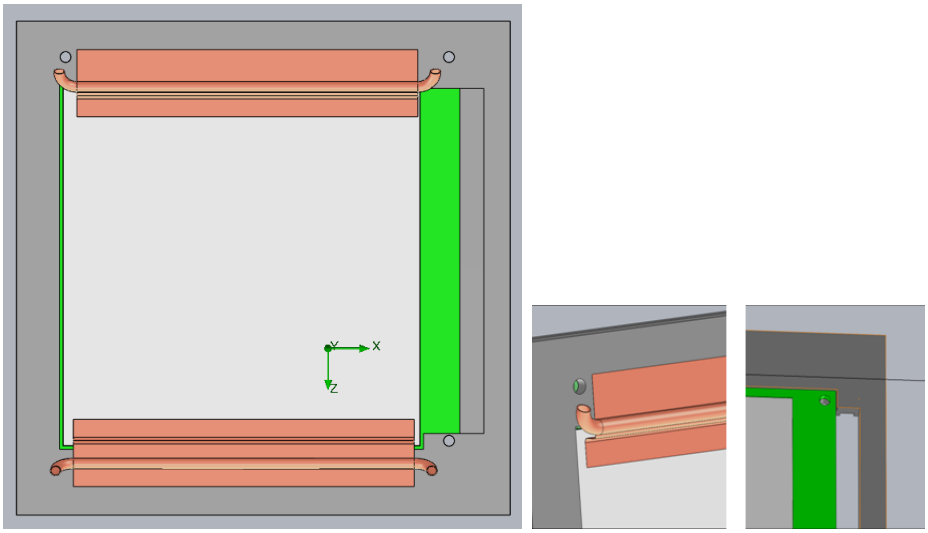

Figure 3.10: CAD pictures of the cooling device *left*: Front view of the cooling device *middle*: view of a bended CU plate *right*: PCB located in the plastic blocks.

The cooling device consists of two quadratic FR4 blocks ($l = 139$ mm, $d_{top} = 5.5$ mm, $d_{bottom} = 3$ mm), which surround the PCB (Figure 4.9 *right*). Mounted on each block are two bent copper plates ($l_{1,top} = 12$ mm, $l_2 = 95$ mm). The copper plates are connected to the silicon wafer through heat conduction pads that are included as a thermal resistance ($\lambda = 2$ W/mK, $d = 0.5$ mm) into the simulation so that the copper plates directly transfer the heat to the wafer. These heat conduction pads isolate voltages up to 10 kV and ensure that the copper plates introduce no short cuts on the silicon wafer. The copper plates are located parallel to the strips of the wafer.

This type of construction may cause that parts of the active area becomes inactive and thus some read-out channels are unusable. To minimize this loss, the contact area ($l_{conact-area}$ = 3.5 mm) is kept as small as possible. Every copper panel introduces a loss of about 5 mm of the active area, leading to about 7 inactive stripes ($N_{channel}$ = 5 mm / d_{pitch} = 5 mm / 0.775 mm $\approx$ 6.5). Overall 28 read-out channels become unusable. This assembling minimizes the temperature gradient, because the two copper plates on the top are perpendicular to the plates of the bottom of the detector. Therefor the wafer is cooled from all four sides. The copper plates are 0.1 mm thin that they do not apply to much pressure on the wafer.
Like in the simulation before, the silicon detector is located in a vacuum pipe. The outer side of the vacuum pipe is again set to 20°C and Propan is used as cooling liquid at a temperature of −15°C. The glue between the silicon wafer and the PCB is included in the simulation as a thermal resistance (λ = 0.18 W/mK, d = 100 m). Moreover heat is exchanged through heat radiation between the elements.

3.3.2 Results of the thermal simulations

Fig. 3.11 shows a homogeneous temperature distribution on the detector due to the cooling from all four sides. The temperature of the silicon wafer is around -10°C as one can see from the temperature scale. All in all there are only little losses.

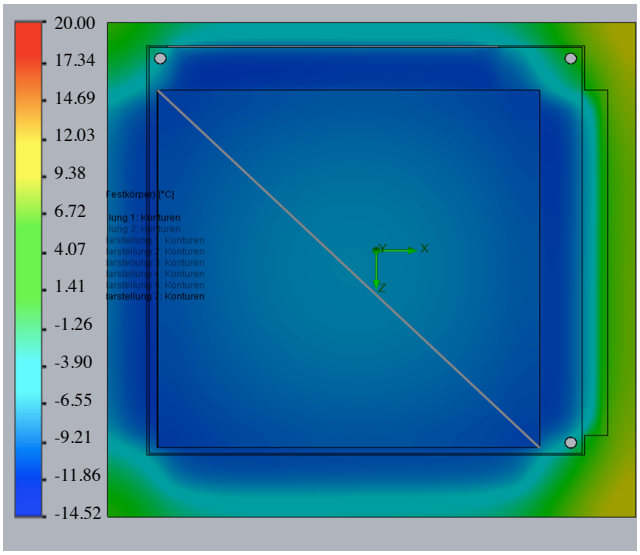

Figure 3.11: CAD picture of temperature distribution on the detector during cooling.

In Fig. 3.12 the temperature is plotted against the length of the diagonal (see Fig. 3.11: grey line) on the silicon wafer. One can see the temperature gradient along the diagonal, which is caused by head radiation. The temperature gradient rises slowly and has its maximum right in the middle of the diagonal at a temperature of about -8°C.

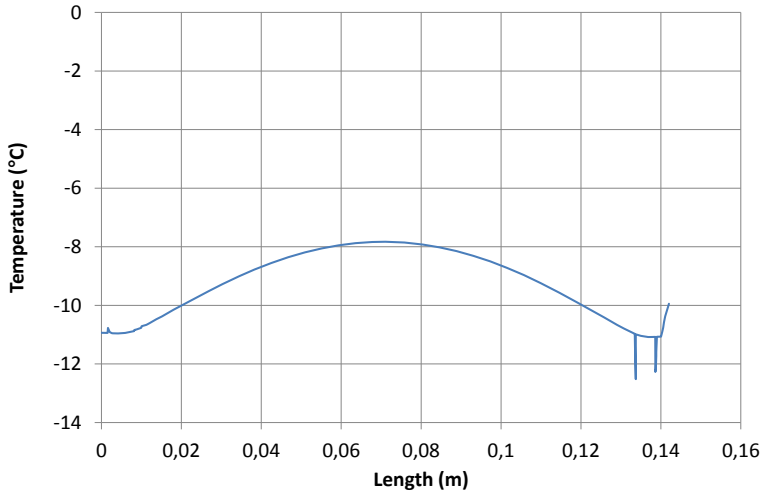

Figure 3.12: Temperature gradient along a diagonal (Fig. 3.11: grey line) through the silicon wafer.

	Minimum	Maximum	Average
silicon wafer	-11.3°C	-7.84°C	-9.35°C
PCB	-12.29°C	5.25°C	-9.94°C

Table 3.5: Temperature of the silicon wafer and the PCB caused by the direct cooling device.

As one can see from Fig. 3.12 and Table 3.5 the heat gradient in the wafer is very small and there are only few losses. Moreover the low heat conductivity of the PCB causes a bigger temperature gradient.
However the temperature of the silicon wafer should be lower than the temperature of the PCB, because FR4[1] has a bigger thermal expansion coefficient than the silicon. If the PCB is cooler than the silicon wafer it carries out pressure on the wafer. Too much pressure could break the silicon wafer.

[1] FR4 is the material of the PCB.

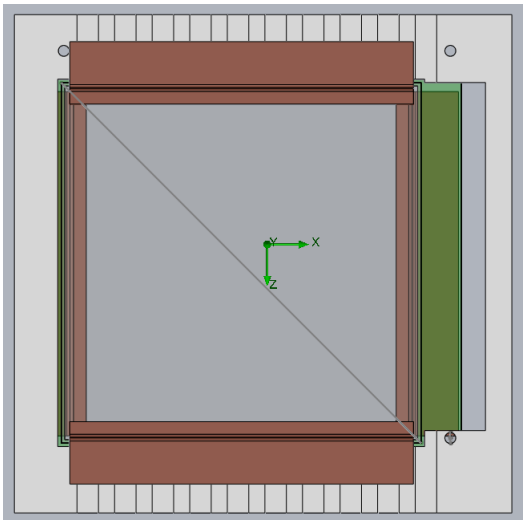

Figure 3.13: CAD picture of plastic board with striation.

In order to avoid the PCB to cool down so much, striation (b_{gap} = 6 mm, $b_{distance}$ = 4 mm, d = 1.5 mm) are embedded into the plastic boards (Fig. 3.13). The PCB is cooled through the silicon wafer and the plastic boards. By minimizing the contact surface of the copper plates on the plastic boards, the plastic boards and therefor the PCB must be warmer.

The temperature distribution of the silicon wafer using the cooling device with the striation is also homogeneous, as one can see in Fig. 3.14. The silicon wafer has nearly the same average temperature like in the simulation above, which is about -10°C.

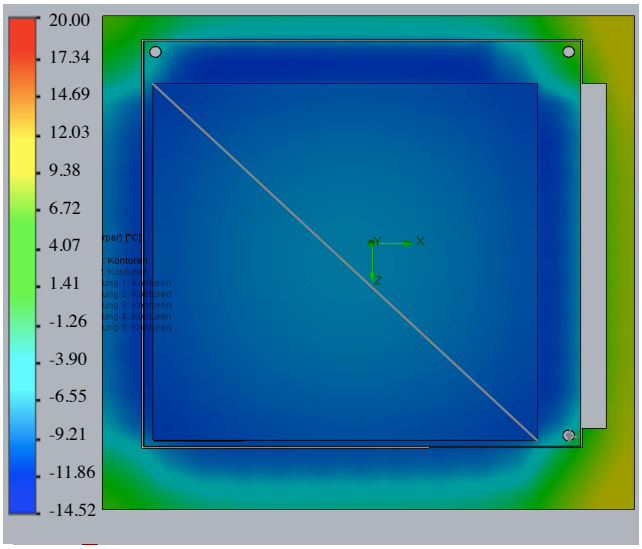

Figure 3.14: CAD picture of temperature distribution the detector, if the plastic boards of the cooling device have gaps on their surface..

Also the temperature gradient along the diagonal (Fig. 3.14: grey line) on the silicon wafer looks quite the same as in the simulation before.

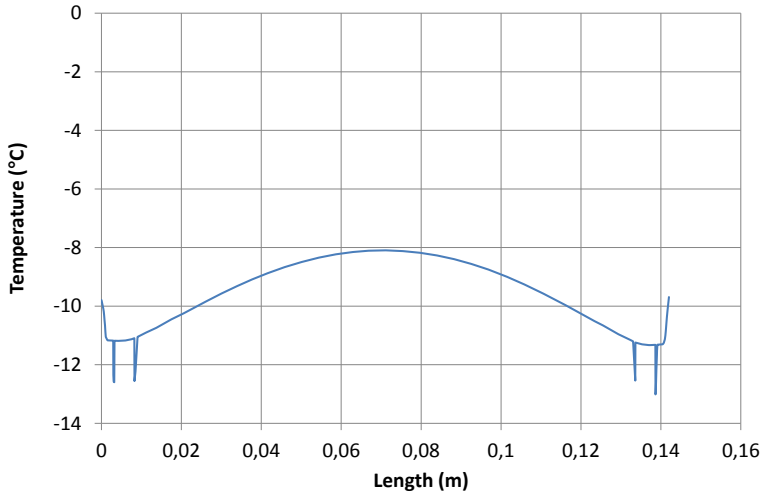

Figure 3.15: Temperature gradient along a diagonal (Fig. 3.14: grey line) through the silicon wafer, if the plastic boards of the cooling device have striation on their surface.

	Minimum	Maximum	Average
silicon wafer	-11.53°C	-8.08°C	-9.60°C
PCB	-12.75°C	6.39°C	-9.89°C

Table 3.6: Temperature of the silicon wafer and the PCB, if the plastic boards of the cooling device have gaps on their surface.

Comparing the average temperatures of the silicon wafer with and without the striation only small difference ($\Delta T_{average} = 0.25°C$) can be seen. The same accounts for the PCB ($\Delta T_{average} = 0.05°C$). Hence the device is not really an improvement and therefor the striation are not an option.

To reduce the pressure on the wafer caused by the mechanical structure, the copper plates are replaced by plates made of brass. Brass is more flexible, and thus the plates act like a spring, which provides still a good heat contact between itself, the heat conduction pad and the silicon wafer.

	Minimum	Maximum	Average
silicon wafer	-10.13°C	-6.65°C	-8.12°C
PCB	-11.93°C	5.50°C	-9.46°C

Table 3.7: Temperature of the silicon wafer and the PCB, if copper plates are replaced by plates made of brass.

Replacing the copper plates with the brass plates does not change the average temperature ($\Delta T_{silicon} = 1.23$°C, $\Delta T_{PCB} = 0.48$°C) notably. From now on the brass plates are part of the direct cooling device.

3.4 Investigation of thermal stress

The results of the thermal simulation can be included in a static simulation to investigate the stress introduced by the temperature gradient and the different thermal expansion coefficients of the materials.

	Si	FR4	Cu
α_T [1/K]	$2.6 \cdot 10^{-6}$	$1.6 \cdot 10^{-5}$	$2.4 \cdot 10^{-5}$

Table 3.8: Thermal expansion coefficients of the materials that are included in a static simulation.

The thermal expansion coefficient α_T connects a uniform temperature change with the strain ϵ_T of the material:

$$\epsilon_T = \frac{\Delta l}{l} = \alpha_T \cdot t, \tag{3.1}$$

where t represents the difference in temperature. If a material is heated up, t is positive, and negative if a material is cooled down.[6]

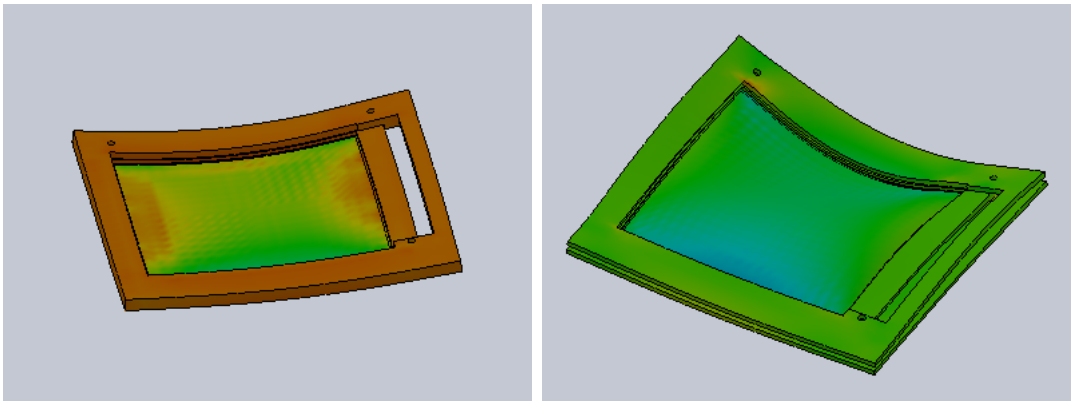

Figure 3.16: CAD picture of deformation due to the cooling with a deformation scaled up by a factor of 44.2553 *left*: direct cooling device *right*: indirect cooling device.

Normal stress is introduced, if a force acts perpendicular on a surface:

$$\sigma = \frac{dF_{\perp}}{dA}. \tag{3.2}$$

The normal stress can be of two types: tensile stress ($\sigma > 0$) and compressive stress ($\sigma < 0$). The tensile strength is the maximum tensile stress and the compressive strength is the maximum compressive stress a material can sustain.[6]

In the proportional range where the deformation is elastic, normal stress (σ) rises linear with strain (ϵ)[6]:

$$\sigma = \epsilon \cdot E. \tag{3.3}$$

Silicon is a hard and brittle material which deforms elastically without any plastic deformation below 500°C. It abruptly breaks if it reaches is yield strength. The yield strength for silicon without defects is about 7 GPa and the Young Modulus E is about 160 GPa. In this case of silicon yield and tensile strength are the same. However little defects in the crystal minimize these values.[9]

The thermal simulation of the direct cooling device with brass plates form the basis of this static simulation. Only the plastic boards, the PCB and the silicon wafer are part of this static simulation. The brass plates and copper pipes are not taken into account.

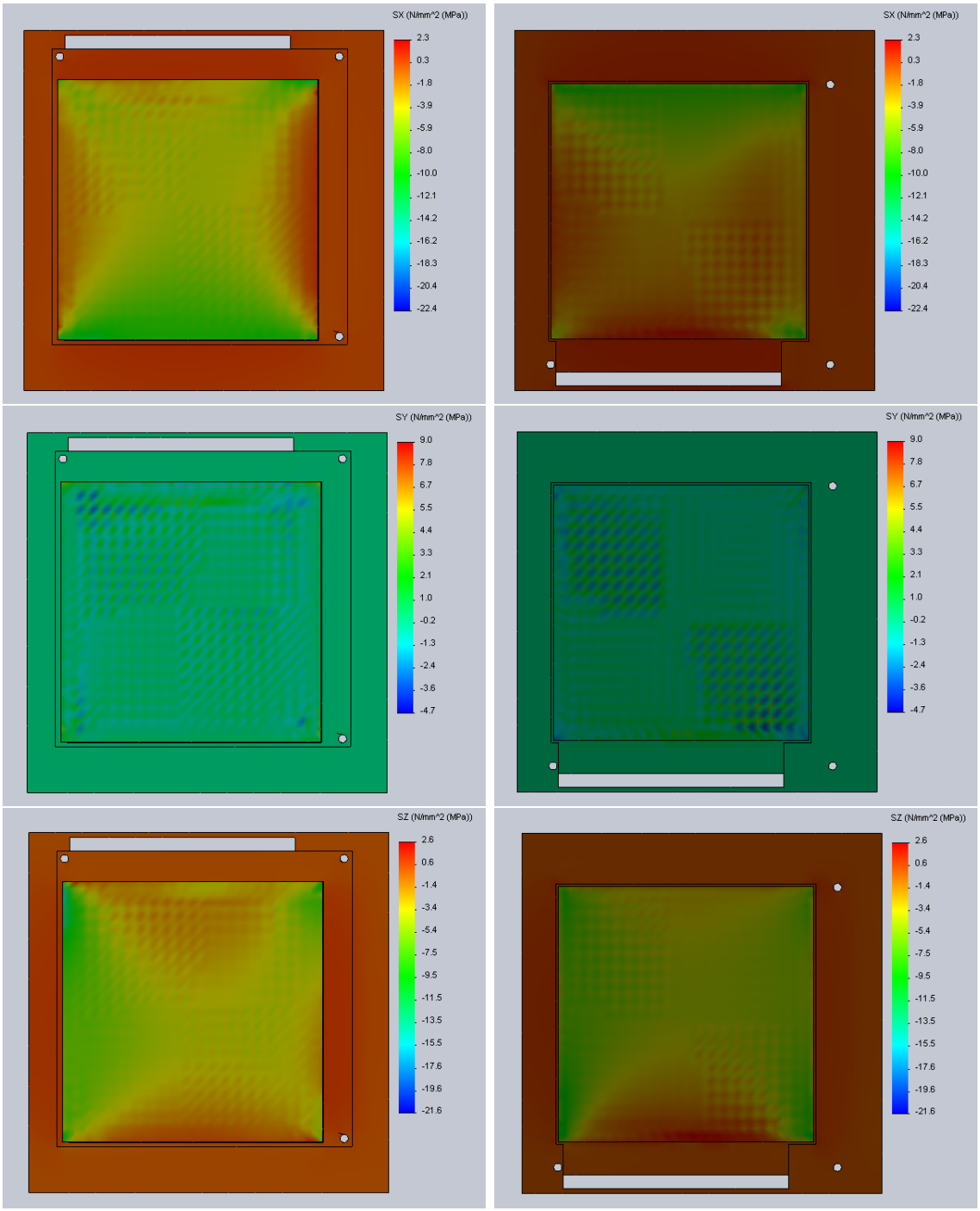

Figure 3.17: CAD picture of normal stress distribution in all three directions caused by the direct cooling device *left*: front-side *right*: back-side.

The underlying thermal simulation of the indirect cooling device for the following static simulation is the one in which only the glue and not the heat source is taken into account. In this static simulation only the copper boards, the PCB and the silicon wafer are included. The copper pipe is neglected.

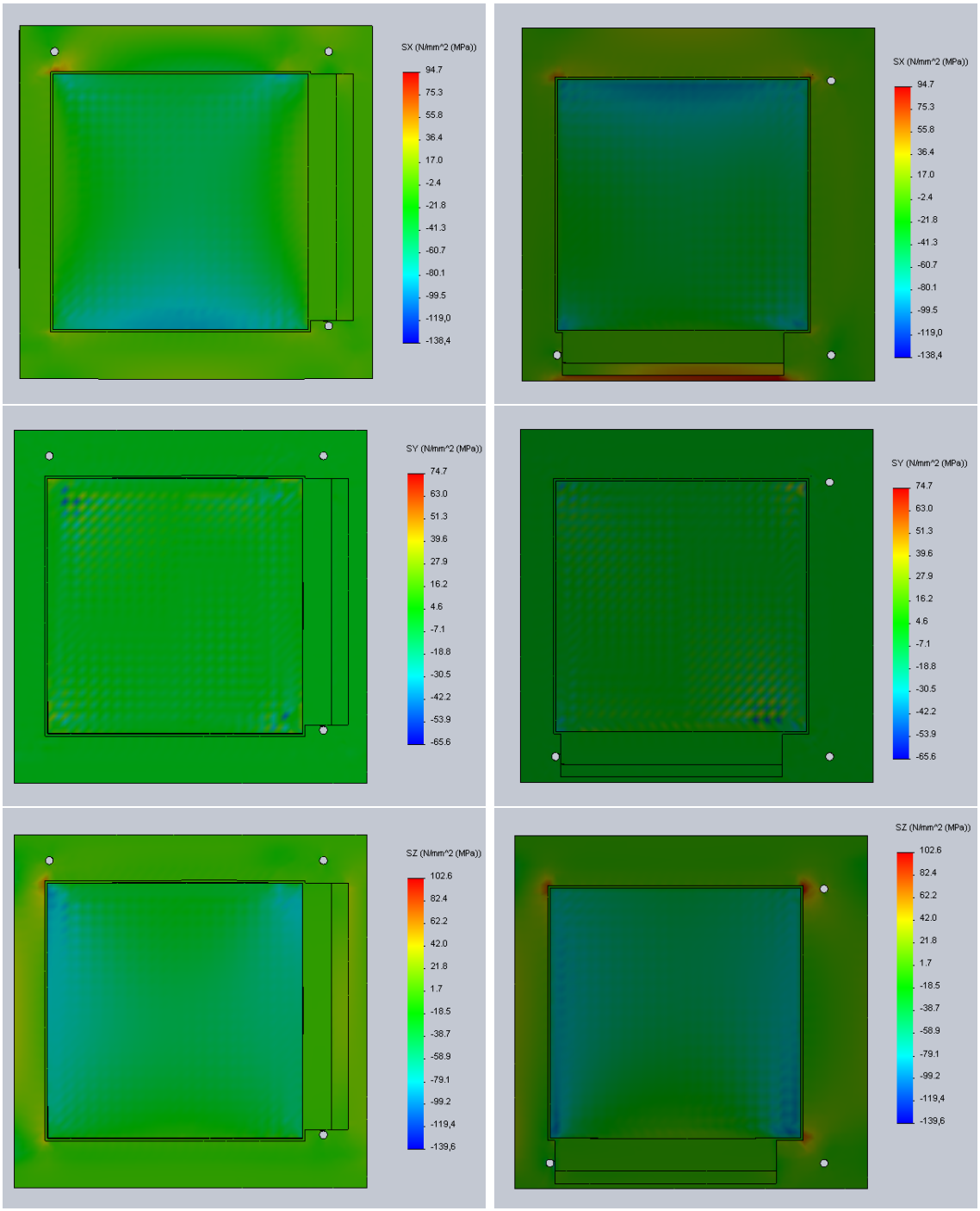

Figure 3.18: CAD picture of normal stress distribution in all three directions caused by the indirect cooling device *left*: front-side *right*: back-side.

	tensile stress	compressive stress
direct cooling device	9.0 MPa	22.4 MPa
indirect cooling device	102.6 MPa	139.0 MPa

Table 3.9: Maximal values of normal stress introduced on the model by the direct and indirect cooling device. The model conists of the PCB, silicon wafer and the plastic boards.

Comparing the normal stress of both cooling systems, normal stress of the direct cooling device is an order smaller. In both cases the compressive stress is higher than the tensile stress due to the fact that the materials contract during cooling (Table 3.9). With the indirect cooling model the compressive stress on the silicon wafer is more dominant as one can see in Fig. 3.18. In contrary to the direct cooling model in which the silicon wafer experienced more tensile stress (Fig. 3.17). In this arrangement tensile strength henpecks. Both maximal values of tensile stresses of the whole model are far below the yield strength of silicon (7 GPa) as one can see from Table 3.9. The value of the yield strength is for a crystal structure with defects smaller, to prevent the silicon wafer from breaking the stress should be kept as small as possible.

3.5 Summary and Outlook

Cooling strongly improves the lifetime and performance of silicon detectors. It reduces the leakage current ($I(-10°\mathrm{C}) = 0.064 \cdot I(20°\mathrm{C})$) and thus guards from thermal runaway. Beyond that reverse annealing is suppressed, if the silicon wafer has a temperature lower than 0°C.
The results of the thermal simulations with the direct cooling device are quite promising. The temperature of the silicon wafer is low and there are only little thermal losses that are partly caused by the absorption of heat radiation in silicon. In reality the heating due to heat radiation is less, since the absorption coefficient α of silicon depends on the wavelength, which is not included into thermal simulations in SolidWorks.
Beyond that the application of the direct cooling device makes sure that the stress attached on the silicon wafer, as a consequence of the temperature gradient and the different thermal expansion coefficients of the materials, is lower compared with the stress of indirect cooling device.
The next step of the development of the cooling system for the silicon detector is to test with silicon wafer dummies if the cooling with the direct cooling device is possible. It has to be investigated, if the brass plates are thin enough, and thus do not apply to much pressure on the wafer. Moreover the whole cooling system has to be built up. That includes the connectors between the cooling pipes and the cryothermostats with regards to the arrangement in the vacuum pipe. It is planned to use the cooling system as soon as possible for a better performance of the silicon detectors during the beam time.

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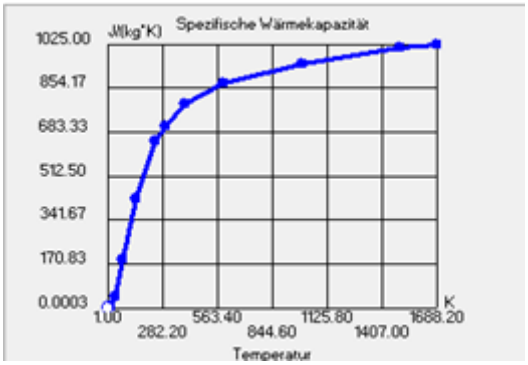
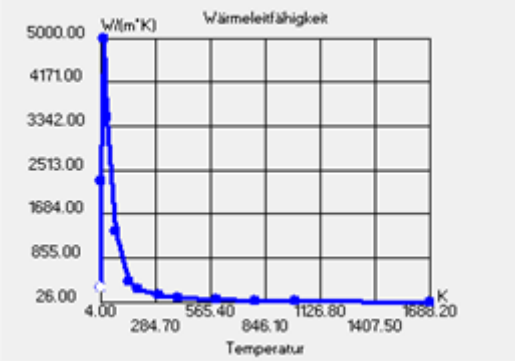
Appendix

Material Properties

- **Silicon**
  - ρ: 2330 kg/m^3
  - specific heat capacity:

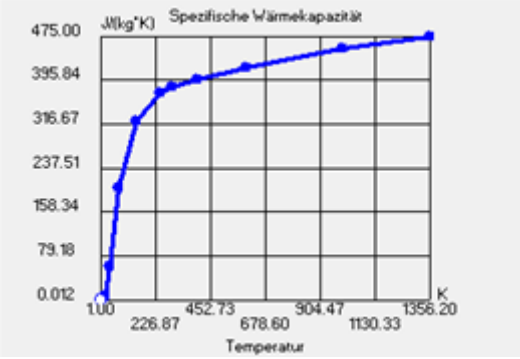


  - heat conductivity:

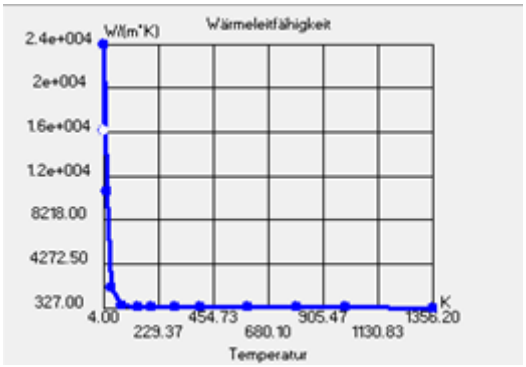


- **FR4**
  - ρ: 1200 kg/m^3
  - specific heat capacity: 880 $J/(kgK)$
  - heat conductivity: 0.3 $W/(mK)$

- **Copper**
  - ρ: 8960 kg/m^3
  - specific heat capacity:

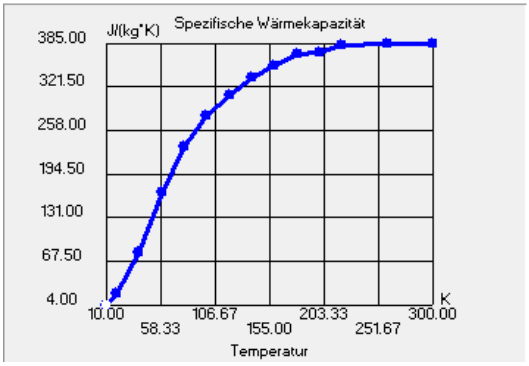


  - heat conductivity:



- **Stainless steel**
  - $\rho = 8000\ kg/m^3$
  - specific heat capacity: 500 $J/(kgK)$
  - heat conductivity: 16.3 $W/(mK)$

- **Brass**
  - ρ: 8400 kg/m^3
  - specific heat capacity:



  - heat conductivity: